XScale PXA250 Target Board

Ordering code	ITPXA250
Dimensions (WxL)	81.4 x 55.5 mm

Introduction

This document describes the XScale PXA250 Target Board. It has been designed for test purposes and for demonstrating the development system.

The board implies Intel XScale PXA250 processor, 1MB Flash and 512kB SRAM memory, a debug JTAG connector, a power supply connector, three LEDs and a reset button.

The user may debug the application and program the flash memory.

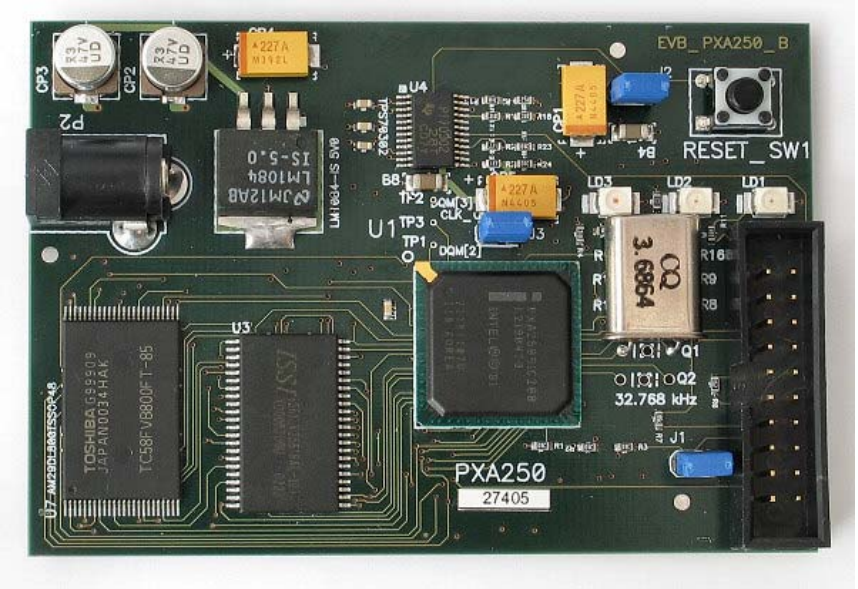

Figure 1: XScale PXA250 Target Board

Board description

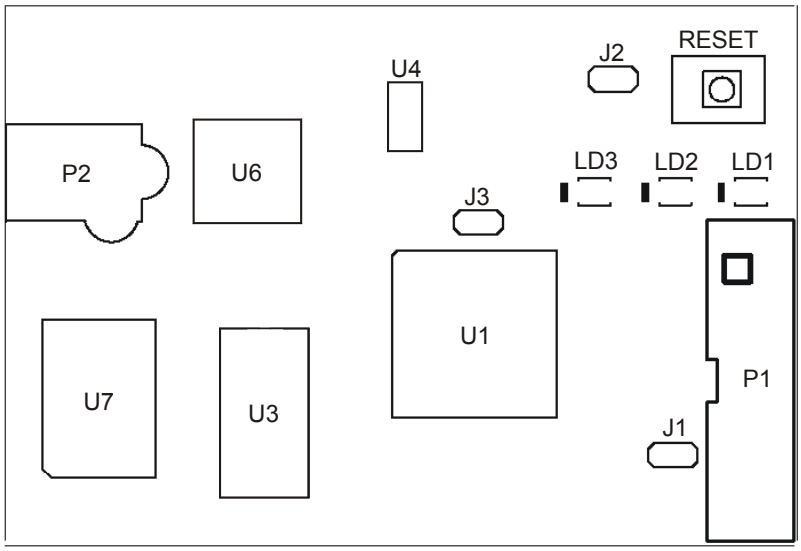

Figure 2: Board description (top side)

Name	Description
U1	Intel XScale PXA250 CPU
U3	SRAM Toshiba TC55V16256
U4	LDO voltage regulator
U6	LDO voltage regulator (5V)
U7	FLASH Toshiba TC58FVB800
P1	JTAG debug connector
P2	Power supply connector
J1	POR jumper
J2	VCCN voltage jumper
J3	VCC voltage jumper
LD1	User LED
LD2	User LED
LD3	Power LED
RESET	Reset push-button

Figure 3: Designator description

JTAG debug connector

VCC	1	2	NC
nTRST	3	4	GND
TDI	5	6	GND
TMS	7	8	GND
TCK	9	10	GND
GND	11	12	GND
TDO	13	14	GND
nRESET	15	16	GND
NC	17	18	GND
NC	19	20	GND

Figure 4: P1 connector pinout

Name	Description
nTRST	JTAG Reset
TDI	JTAG Data Input
TMS	JTAG Mode Select
TCK	JTAG Clock
TDO	JTAG Data Output
nRESET	CPU Reset
VCC	+3.3 V
GND	Ground
NC	Not connected

Figure 5: P1 pin description

Power supply

The external power supply must provide the voltage between 6 and 12V DC and the power of approx. 200mW, the polarity is not important, just the low voltage DC plug must conform to the DIN 45323 standards:

- the hole diameter is 1.95 – 2.5 mm (standard: 2.1 mm)
- the external diameter is 6.2 - 5.5 mm (standard: 5.5 mm)

See the following picture for dimensions:

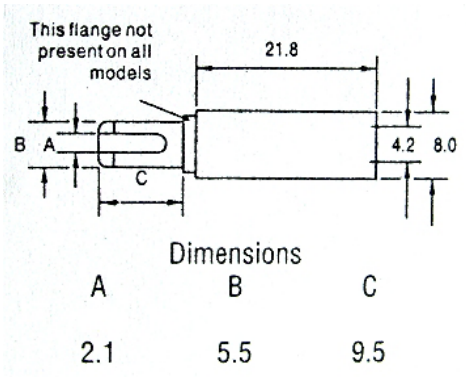

Figure 6: DC plug dimensions

Note: The emulator must be powered on first, then the target board and vice versa when switching off the system. First, switch off the target and then the emulator.

Jumpers

There are three jumpers on the board: jumper J1 configures Power on Reset, generated by LDO voltage regulator U4; jumpers J2 and J3 configures I/O and core voltages.

J1	**Use POR (Power on Reset)**
ON	Enable (DEFAULT)
OFF	Disable
J2	**3.3V I/O voltage**
ON	Enable (DEFAULT)
OFF	Disable
J3	**1.8V core voltage**
ON	Enable (DEFAULT)
OFF	Disable

Figure 7: Jumper configuration

Indicators

Three LEDs (LD1, LD2 and LD3) are available on the board. LD1 and LD2 are connected to GPIO pins 3 and 4 of the CPU and can be switched on/off by the target application. LD3 indicates presence of power supply (+3.3V).

Reset button

Reset push-button (RESET_SW1) resets the target.

Bill of material

Part	Value	No.
B1	1μF	2
B2-B4	100nF	30
B5	1μF	/
B6-B32	100nF	/
CP1	220μF	3
CP2	33μF/35V	2
CP3	33μF/35V	/
CP4	220μF	/
CP5	220μF	/
J1	JMP2	3
J2	JMP2	/
J3	JMP2	/
LD1	LED RED	2
LD2	LED RED	/
LD3	LED GREEN	1
P1	IDC20TH	1
P2	POWERJACK	1
R1-R4	10k	9
R5	0E	1
R6	1k5	2
R7	75E	1
R8	10k (0805)	3
R9, R10	100k (0805)	3
R11,R12,R13	330E	3
R14	100k (0805)	/
R15,R16	10k (0805)	/
R17,R18,R19	10k	/
R20	1k5	/
R21,R22	220E	2
R23,R24	10k	/
RESET_SW1	PUSH-5X5P	1
Q1	3.6864 MHz	1
Q2	32.768 kHz	1
U1	XScale PXA250	1
U3	TC55V16256	1
U4	TPS70302	1
U5	DF15005S	1
U6	LM1084-IS 5V0	1
U7	TC58FVB800	1

Schematic

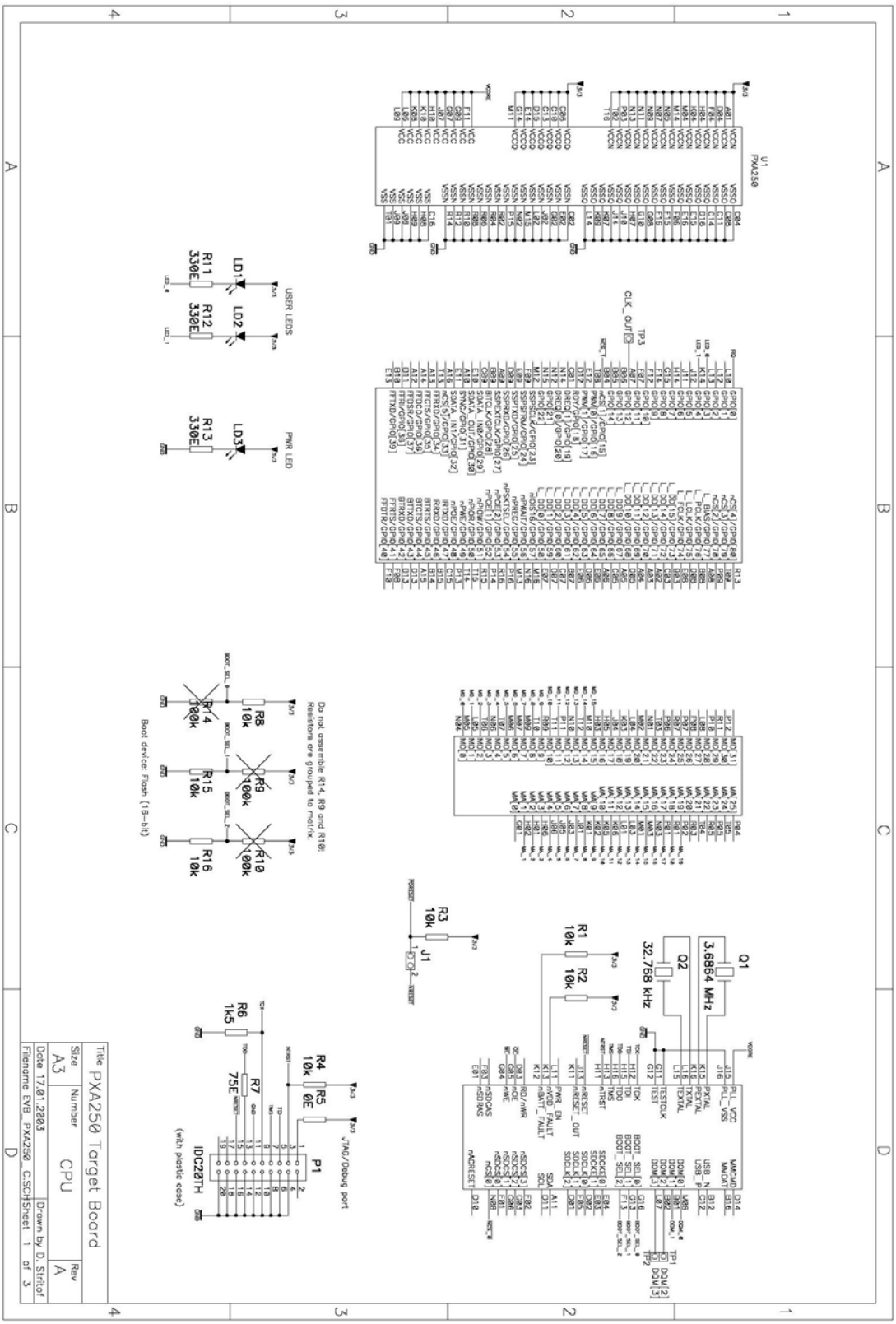

Figure 8: Schematic - CPU

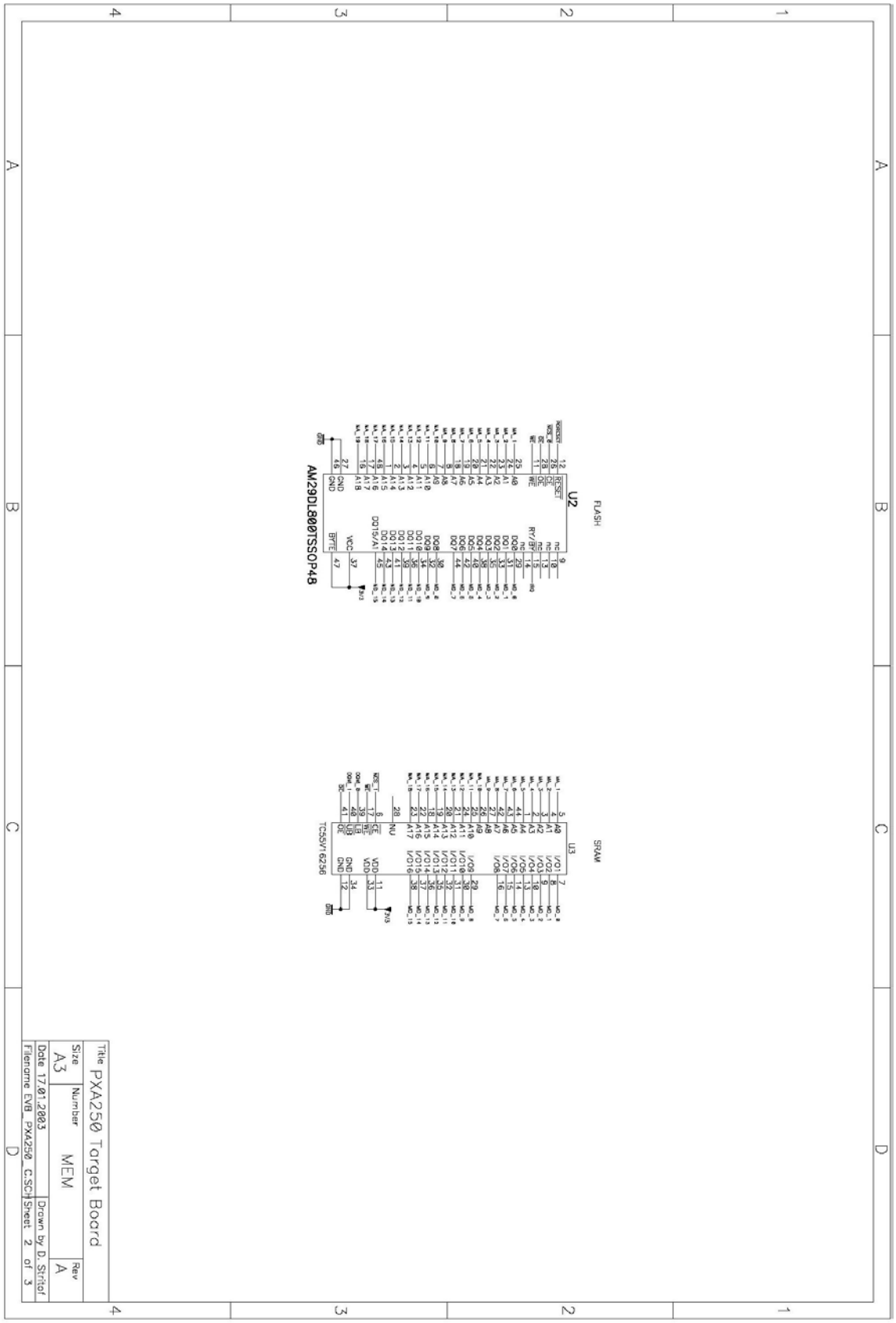

Figure 9: Schematic - Memory

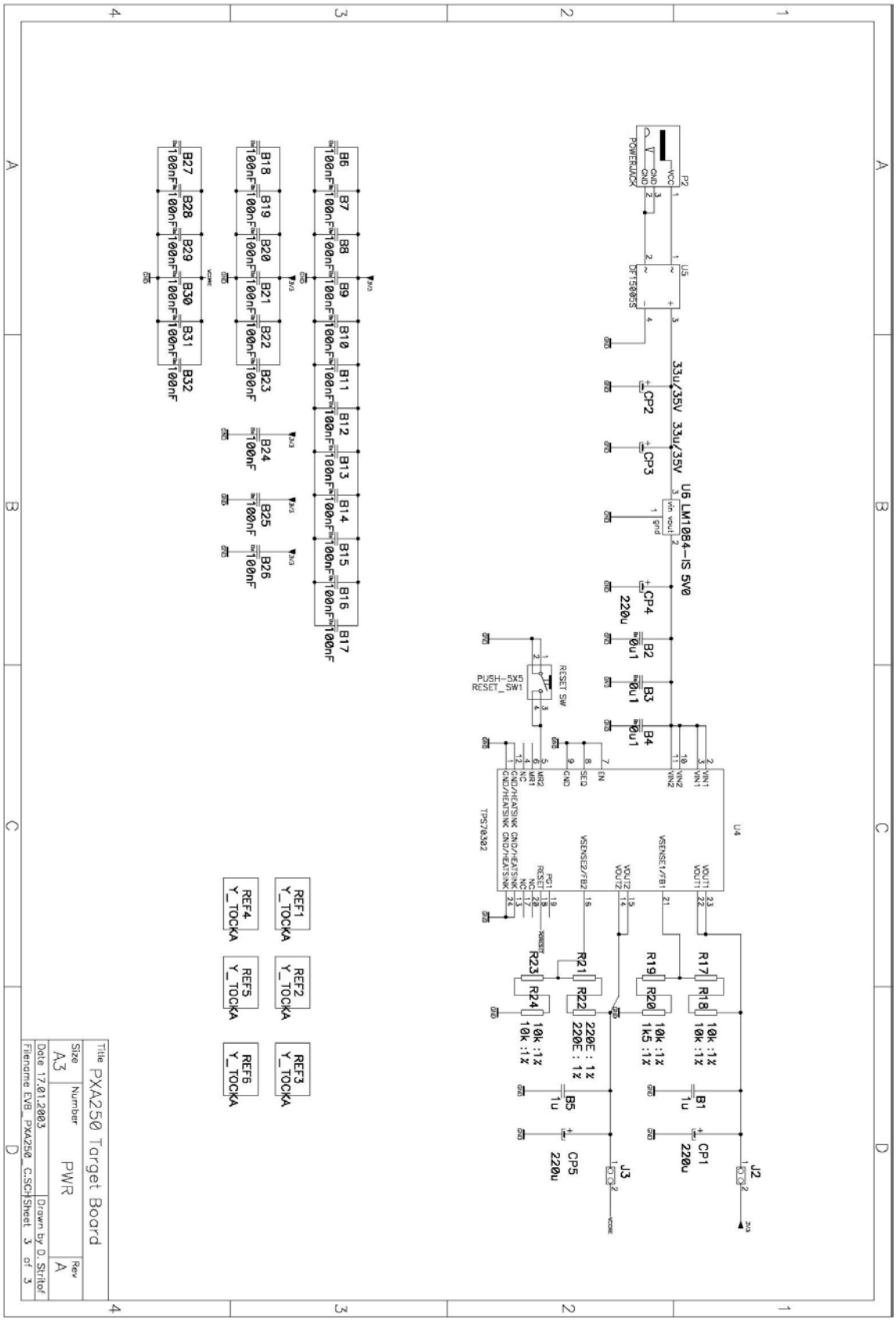

Figure 10: Schematic - Power supply