NEC V850ES/Fx3 Target Board

Ordering code	ITV850Fx3
Dimensions	123 x 63 mm

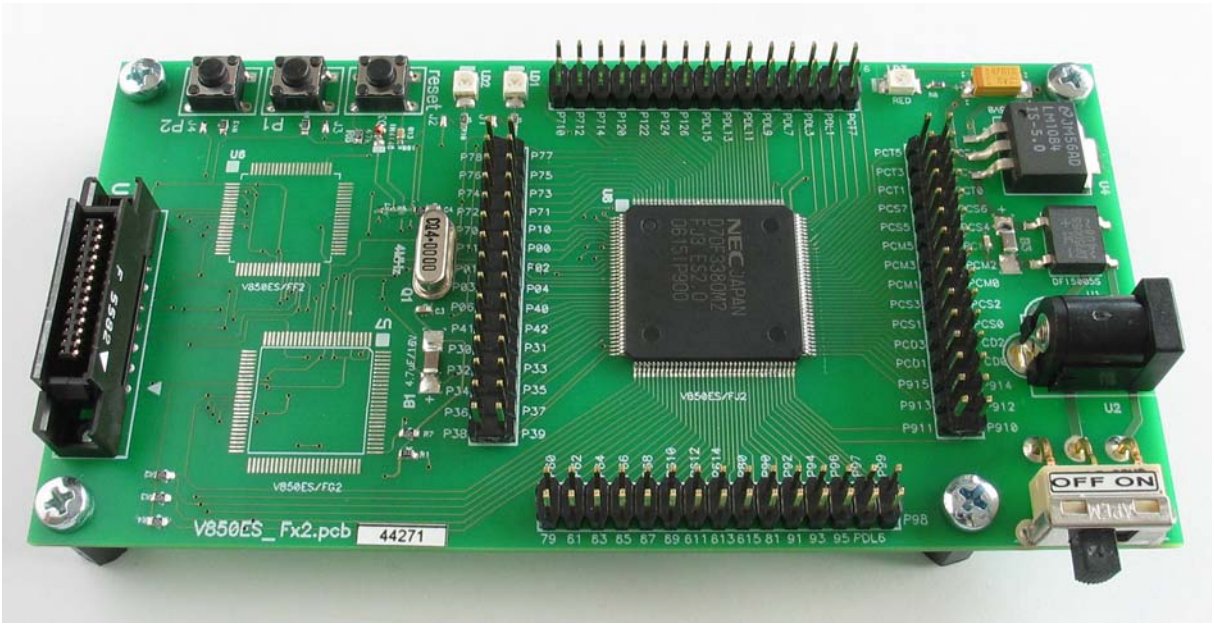


Figure 1:V850ES/Fx3 Target Board

Contents

Introduction

V850ES/Fx3 Target Board is an evaluation and a development system for NEC V850ES/Fx3 based microcontrollers and is populated with μPD70F3380 CPU.

Description

View of the V850ES/Fx3 Target Board

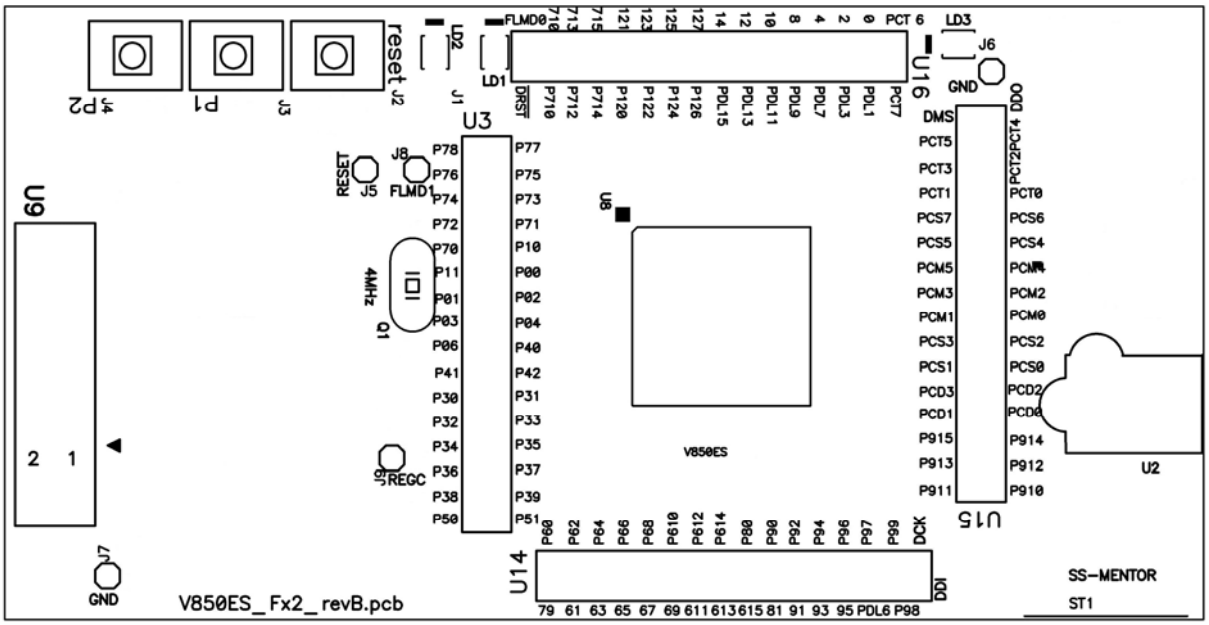


Figure 2: Top View of the V850ES/Fx3

Block Diagram

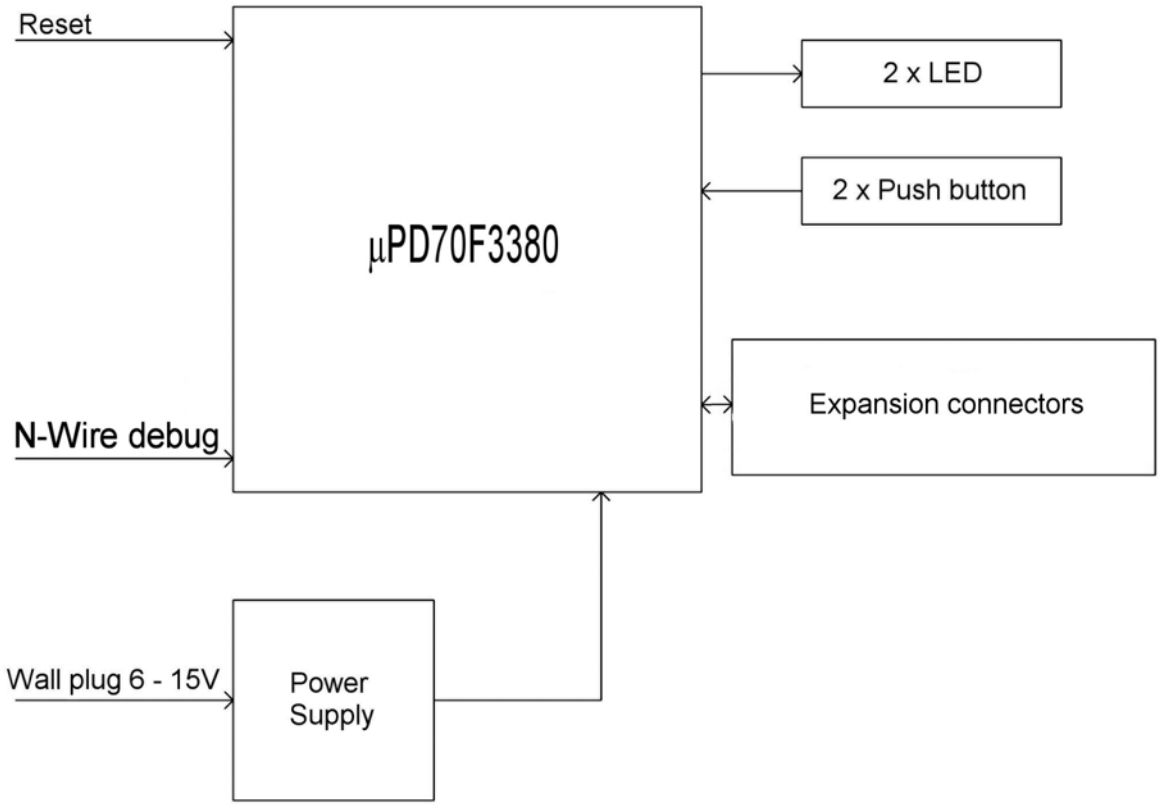


Figure 3: Block diagram V850ES/Fx3

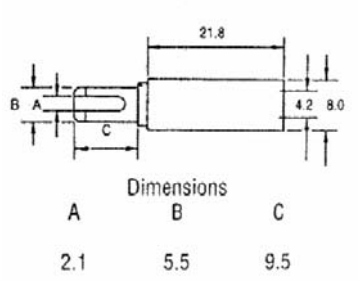
Components List

Name	Description
P1	Push button
P2	Push button
J10	Jumper
LD1	LED
LD2	LED
LD3	Power supply LED
Reset	Reset button
Q1	4 MHz crystal oscillator
U2	Power supply jack
U8	Solder pattern for µPD70F3380
U9	N-Wire debug connector
ST1	Power switch
U3	Expansion connector
U14	Expansion connector
U15	Expansion connector
U16	Expansion connector

Power Supply

Permissible input voltage: 6-15 V DC. A power supply with a minimum of 100mA is recommended. Low voltage DC plug must conform to the DIN 45323 standards:

The hole diameter is 1.95 – 2.5 mm (standard: 2.1 mm)
The external diameter is 6.2 - 5.5 mm (standard: 5.5 mm)



Switch-on the V850ES/Fx3 after the AC adapter is plugged into the wall and connected to the V850ES/Fx3. Check that power indicator LD3 lit, indicating that 5V voltage is present.

Note: When connecting an external debugger, make sure that the emulator is powered on first, then the target board and vice versa when switching off the system. First, switch off the target and then the emulator.

Jumper Descriptions

J1: LD1 Enable: J1 is set to enable LD1 LED. Default set.

J2: LD2 Enable: J2 is set to enable LD2 LED. Default is set.

J3: P1 Enable: J3 is set to enable P1 push button. Default is set.

J4: P2 Enable: J4 is set to enable P2 push button. Default is set.

J10: It must not be populated for normal debugging and a standalone target operation. It must be set only when Hot Attach debug feature is used, which requires 1K pull-up on the CPU DRST line.

26-pin N-Wire debug connector (U9)

Not used	1	2	GND
Not used	3	4	GND
Not used	5	6	GND
Not used	7	8	GND
Not used	9	10	GND
Not used	11	12	GND
DDI	13	14	GND
DCK	15	16	GND
DMS	17	18	GND
DDO	19	20	GND
DRST	21	22	Not used
RESET	23	24	Not used
FLMD0	25	26	+5V

External JTAG debug tool connects to a 26-pin N-Wire debug connector.

CPU expansion connectors

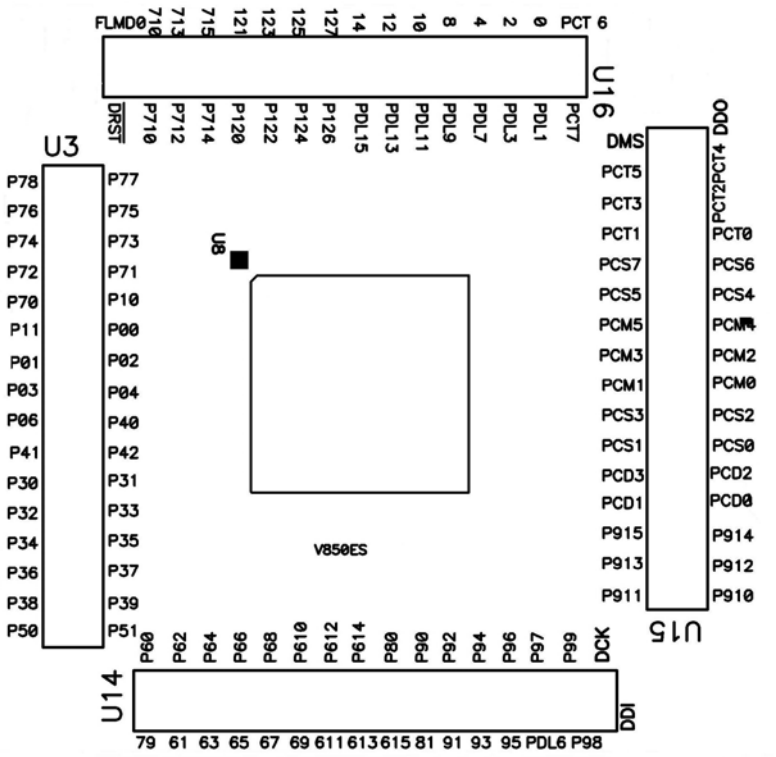
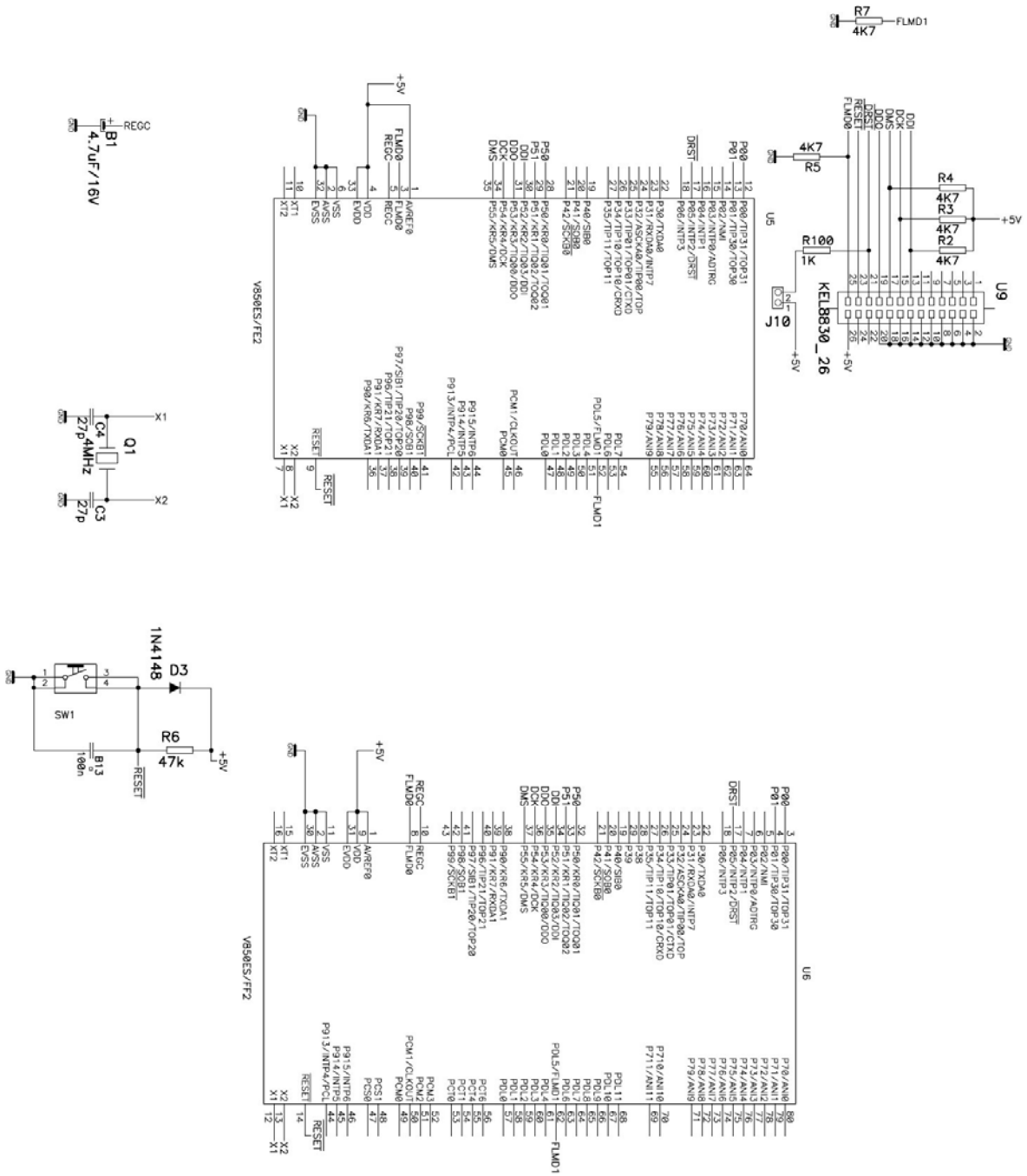


Figure 4: Expansion connectors

Note: The following CPU signals are not available on the expansion connectors: FLMD1, REGC and RESET.

Schematic


R7
4K7
FLMD1
R5
4K7
R100
1K
R4
4K7
R3
4K7
R2
4K7
+5V
U9
KEL8830_26
J10
U5
V850ES/FE2
REGC
B1
4.7uF/16V
C4
27p
4MHz
Q1
C3
27p
X1
X2
RESET
SW1
1N4148
D3
R6
47k
B13
100n
U6
V850ES/FF2