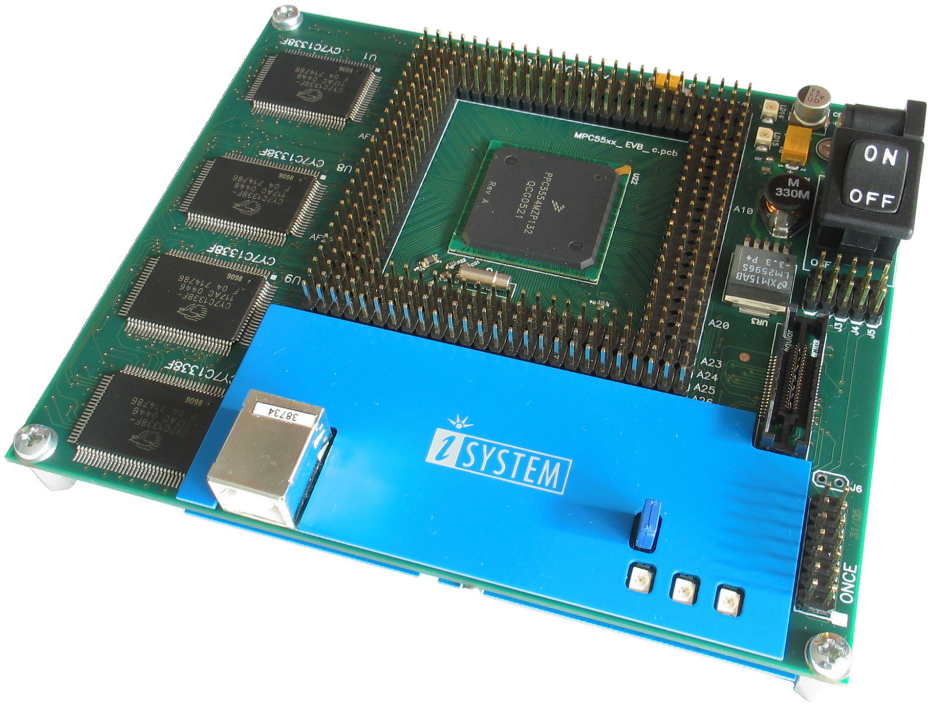
User's Manual

EVB-5566 Evaluation & Development Kit for Freescale PowerPC MPC5566 Microcontroller

	Ordering code
EVB-5566	ITMPC5566



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Contents

Features

The ITMPC5566 Target Board is an evaluation and a development system for the Freescale MPC5566 microcontroller. The ITMPC5566 package consists of a USB cable, a power supply and a target board populated with the Freescale MPC5566 CPU, option of installation of 2 MB SRAM (4 devices 128Kx32-bit, not populated), JTAG debug and Nexus debug connectors and an on-board integrated iSYSTEM JTAG debugger. The application under the development or test runs from the internal CPU flash.

Specifications

Clock Speed – up to 132 MHz
Power requirement: 6 - 12V DC , + in the center @ 500 mA
Power output: 5V, 3.3V, and 2.5V regulated supplies
Board Size: 131 mm x 110 mm

EVB-5566 Features

- MPC5566
- Optional ext. 2Mbit (4 devices 128K x 32-bit) SRAM (CY7C1338F) – not populated
- 8MHz clock (ext. crystal)
- Power Indicators – Supply voltage indications for 5V, 3.3V, and 2.5V supplies
- User Indicator – two user indicators to provide user conceived visual response during testing
- Configuration jumper - Jumpers J1 to J5 configures processor startup mode; Jumper J6 enables/disables the iSYSTEM on-board integrated USB-JTAG debugger
- Two debug options available – JTAG, Nexus
- Low cost and user friendly support manual and software

Software Development

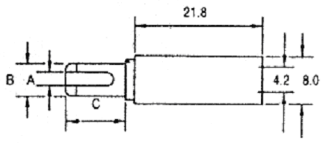
The board has been tested and does run at speeds up to 132 MHz, which you can set by engaging the PLL module in your software. Software development on the EVB-5566 can be performed using the iSYSTEM on-board integrated USB-JTAG debugger. Alternatively, external development tools can be connected to the ONCE (JTAG) or P2 (Nexus) connector. This provides real-time access to all hardware, peripherals and memory on the board. Software is usually uploaded to the external SRAM where it's executed during the development. Then it can be programmed into the CPU Flash in order to execute in standalone when the power is applied.

Getting Started - Setting up the EVB-5566 Board

Power Supply

Permissible input voltage: 6-12 V DC, **+ in the center.** The required current load capacity of the power supply depends on the specific configuration of the ITMPC5566. A power supply with a minimum of 500mA is recommended and delivered in the package. Low voltage DC plug must conform to the DIN 45323 standards:

- The hole diameter is 1.95 – 2.5 mm (standard: 2.1 mm)
- The external diameter is 6.2 - 5.5 mm (standard: 5.5 mm)



Dimensions

A	B	C
2.1	5.5	9.5

Switch-on the EVB-5566 after the AC adapter is plugged into the wall and connected to the EVB-5566. Check that power indicators (LD11, LD12, LD13) lit, indicating that 5V, 3.3V and 2.5V voltage is present.

Note: When connecting an external debugger, make sure that the emulator is powered on first, then the target board and vice versa when switching off the system. First, switch off the target and then the emulator.

Use of On-Board Integrated Debugger

Follow below instructions, in order to get a sample application running with "out of the box" experience.
If winIDEA 2006 CD is not part of the package, please obtain winIDEA 2006 setup from your local iSYSTEM office or from www.isystem.com.

- Install winIDEA 2006 (IDE) full setup on a PC.
- Set jumpers J1-J5 in their default position.
- Set jumper J6, which enables on-board integrated debugger.
- Make sure that power switch on the ITMPC5566 is in off position.
- Connect the power supply to the ITMPC5566.
- Switch on the ITMPC5566.
- Run winIDEA by selecting Start>Programs>… and open ITMPC5566 sample workspace (.jrf) running from the internal flash c:\winIDEA\2006\Examples\Targets\ITMPC5566\IntFLASH).
- Connect USB cable between the PC and the ITMPC5566.
- Windows should auto-detect a new USB device and install belonging USB driver. In case of any problems, the driver is located under winIDEA install directory (e.g. c:\winIDEA\2006\USBDrv).
- Execute Debug/Download. This should program and run the application until main function.
- The application is now ready for debugging. If you run the application, a successful operation is indicated with blinking LED LD11 and LD12.

The on-board integrated USB-JTAG debugger runs without restrictions for 90 days after using it for the first time. After the 90 day period expires, the debugger falls back to a restriction of a 32k byte download limit.

The debugger can be upgraded to a regular debugger (no limits) by purchasing the debug enable license. Additionally, you need to purchase a regular winIDEA license. Please contact your local iSYSTEM distributor for more details on upgrading your development tool.

What To Do Now?

winIDEA allows you to run code step by step, set execution and access breakpoints, examine and modify the source code, rebuild the project using GNU compiler, which is optionally installed during winIDEA installation, and much more. For more information refer to the winIDEA documentation. Software in the combination with the development board can be used as a basis for developing future applications also on your hardware. This project illustrates various programming issues, which are essential to all winIDEA projects:

- Initialization of bus interface unit
- Initialization of configuration registers
- Implementation of dispatch table
- Format of linker definition file
- Correct project settings (Project>Settings), which ensure that the compiler is invoked successfully

More interesting examples are also included on the support CD.

Troubleshooting

EVB-5566 doesn't show signs of life by first start

a) Check the power supplied to the EVB board – Diodes LD11, LD12 and LD13.

b) When using the on-board integrated JTAG debugger, make sure that Jumper J6 is enabled. When Jumper J6 is not enabled, a connection to the JTAG or Nexus port must be made.

c) Try "slow" JTAG Scan Speed if the debugger cannot connect to the CPU.

d) Execute debug Reset instead of debug Download.

Unable to download the code to the board

a) Check the power supplied to the EVB board.

b) Ensure that the correct workspace was loaded into winIDEA.

c) Check the hardware configuration:

- Tools>Hardware Plug-In
- Hardware>Hardware …
- Hardware>Emulation Options

d) Reset the board and try to connect again.

Checksum failed error

a) When performing any kind of checksum, remove all software breakpoints

Default Memory Map

The MPC5566 of the MPC5500 family has two levels of memory hierarchy. The fastest accesses are to the unified 32 Kbytes cache. The next level in the hierarchy contains the 128-Kbyte internal SRAM and internal 3MB Flash memory. Both the internal SRAM and the Flash memory can hold instructions and data. The external bus interface has been designed to support most of the standard memories used with the MPC55xx family. The provided software uses the default memory map. If you modify the memory map make sure that all memory banks and chip select configuration settings are adjusted accordingly.

EVB-5566 Memory Map

Internal Memory

Address Range	Memory Type	Description
0x 0000 0000- 0x 002F FFFF	3MB - Internal Flash Memory	Internal Flash memory
0x 2000 0000- 0x 3FFF FFFF	512MB - External Memory	External Memory (see note below)
0x 4000 0000- 0x 4000 7FFF	Internal SRAM, Powered Standby	32 Kbytes
0x 4000 8000- 0x 4001 FFFF	Internal SRAM	96 Kbytes

External Memory

Optionally, there are 4 SRAM devices connected to CS1 and CS2 and cover a 2MB memory area. Offset depends on the CPU configuration. In our case, CS1 is configured to point at 0x2000 0000 through the winIDEA initialization sequence.

Address Range
0x 2000 0000 – 0x 2007 FFFF
0x 2008 0000 – 0x 200F FFFF
0x 2010 0000 – 0x 2017 FFFF
0x 2018 0000 – 0x 201F FFFF

SRAM Memory

The MPC5566 internal SRAM module provides a general-purpose 128-Kbyte memory block that supports mapped read/write accesses from any master. Included within the 128-Kbyte SRAM block is a 32-Kbyte block powered by a separate supply for a standby operation.

Flash Memory

The MPC5566 provides 3 Mbytes of programmable, non-volatile, Flash memory storage. The non-volatile memory (NVM) can be used for instruction and/or data storage.

Downloading the code into the memory

winIDEA allows you to load the code directly into the internal Flash memory through the standard debug download. winIDEA identifies, which code from the download file fits in the internal FLASH, and loads it to the Flash through the flash programming procedure hidden to the user. All other code propagates to the target through standard memory writes.

Demo software has the example configured for the internal Flash. Load the project into winIDEA and execute debug download (Debug->Download), which will download the code directly to the Flash memory. For more information see the winIDEA users manual.

Demo software has also the example configured for the optionally populated external SRAM. Load the project into winIDEA and execute debug download (Debug->Download), which will download the code to the external SRAM. Access to the external SRAM is configured in the initialization sequence ('Hardware/Emulation Options/Initialization' tab), which winIDEA executes prior to debug download.

Settings and Options

Jumpers

Jumpers J1 to J5 configures processor startup mode. See MPC5566 Reference Manual for more details on the CPU signals BOOTCFG[0:1], PLLCFG[0:1] and WKPCFG. Some boards may not have J1-J5 populated since the CPU has internal pull-ups/downs on belonging signals, which match with the default jumper settings. Jumper J6 selects whether iSYSTEM on-board integrated USB-JTAG debugger is used or an external debug tool.

Jumper pin 1 is marked with a white square on the ITMPC5566 PCB. If pin 1 cannot be located directly from the ITMPC5566, please use Figure 2 for assistance.

Note: Don't change jumper settings while the ITMPC5566 Target Board is supplied with power!

J1	**BOOTCFG0**
1-2*	BOOTCFG0 = 0
2-3	BOOTCFG0 = 1
J2	**BOOTCFG1**
1-2*	BOOTCFG1 = 0
2-3	BOOTCFG1 = 1
J3	**PLLCFG0**
1-2	PLLCFG0 = 0
2-3*	PLLCFG0 = 1
J4	**PLLCFG1**
1-2	PLLCFG1 = 0
2-3*	PLLCFG1 = 1
J5	**WKPCFG**
1-2	WKPCFG = 0
2-3*	WKPCFG = 1
J6	**Debug mode**
Closed*	Enable integrated USB-JTAG debugger
Open	External debugger

Figure 1: Jumper configuration (* - default position)

Status Indicators

Three LED diodes show the presence of supply voltages. LD11 (+5V), LD12 (+3.3V) and LD13 (+2.5V) must light when the power is applied to the evaluation board. LD14 and LD15 are available for the user as a status indicator.

Component List

Name	Description
U22	Motorola MPC5566 CPU
U1,U8,U9,U10	SRAM Cypress CY7C1338F
P1(bottom)	Connector for manufacturing purpose
P2	Nexus debug connector
P4	Power supply connector
ONCE	JTAG debug connector
J1	BOOTCFG0
J2	BOOTCFG1
J3	PLLCFG0
J4	PLLCFG1
J5	WKPCFG
J6	Debug mode
J28	USB connector (integrated debugger)
LD11	Power LED 5V
LD12	Power LED 3,3V
LD13	Power LED 2,5V
LD14	User LED
LD15	User LED
SW1	Power switch

Connectors

14-pin JTAG debug connector (ONCE)

CPU_TDI	**1**	**2**	GND
CPU_TDO	**3**	**4**	GND
CPU_TCK	**5**	**6**	GND
N.C.	**7**	**8**	N.C.
CPU_RESET	**9**	**10**	CPU_TMS
3V3	**11**	**12**	N.C.
N.C.	**13**	**14**	CPU_TRST

External JTAG debug tool connects to a 14-pin JTAG debug connector. **Jumper J6 must be open when using external debugger.**

Nexus 38-pin Mictor debug connector

Signal	Pin	Pin	Signal
Not used	1	2	Not used
Not used	3	4	Not used
MDO9	5	6	CLKOUT
BOOTCFG	7	8	MDO8
RSTIN	9	10	EVTIN
TDO	11	12	VTREF
MDO10	13	14	RDY
TCK	15	16	MDO7
TMS	17	18	MDO6
TDI	19	20	MDO5
NTRST	21	22	MDO4
MDO11	23	24	MDO3
Not used	25	26	MDO2
Not used	27	28	MDO1
Not used	29	30	MDO0
Not used	31	32	EVTO
Not used	33	34	MCKO
Not used	35	36	MSEO1
Not used	37	38	MSEO0

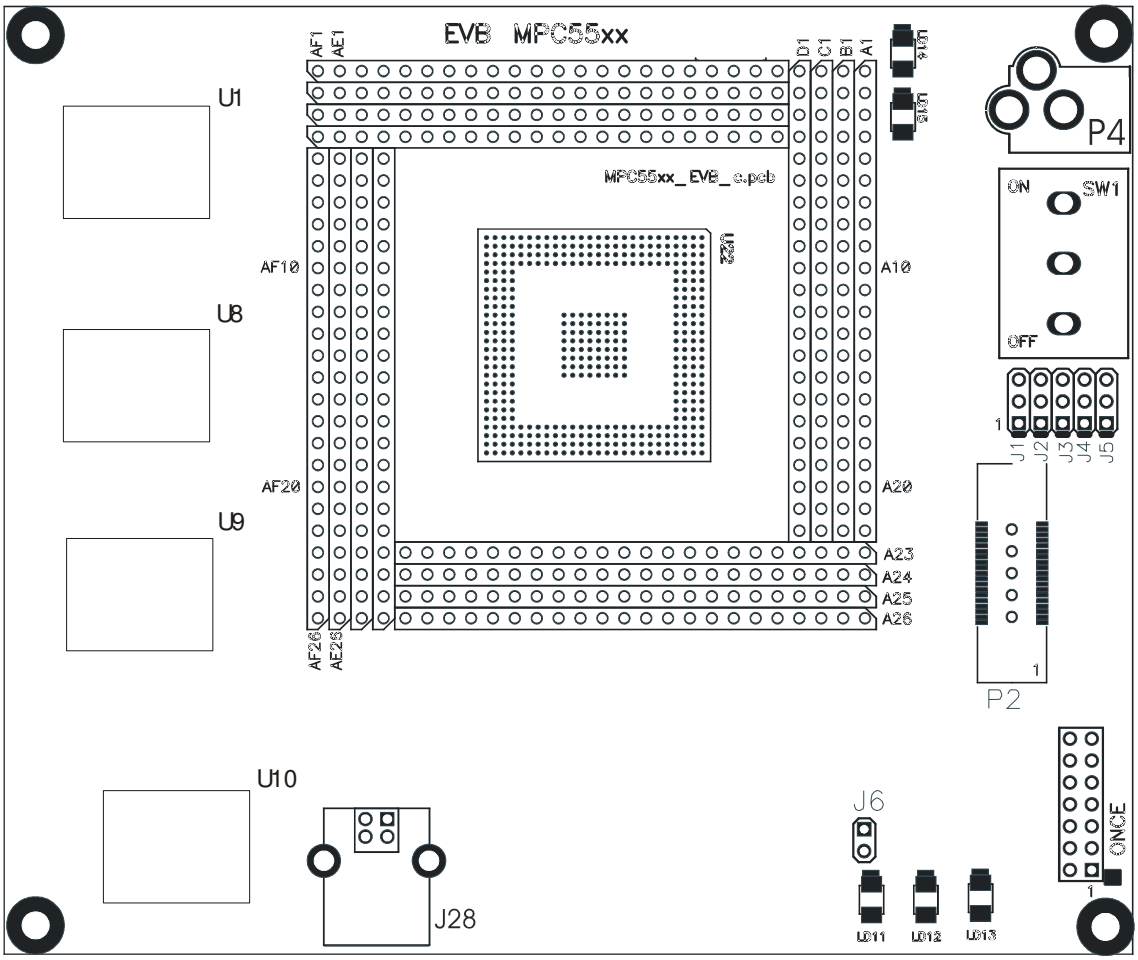
External Nexus debug tool connects to a Nexus 38-pin Mictor debug connector. **Jumper J6 must be open when using external debugger.**

CPU expansion connector

The CPU expansion connector makes all the CPU signals accessible and can be used in order to expand the development system by connecting the ITMPC5566 to another module. The CPU expansion connector uses the same numbering scheme as the original CPU in the PBGA416 package. The CPU expansion connector builds the matrix that matches with the CPU PBGA416 pinout.

Appendix A

View of the ITMPC5566



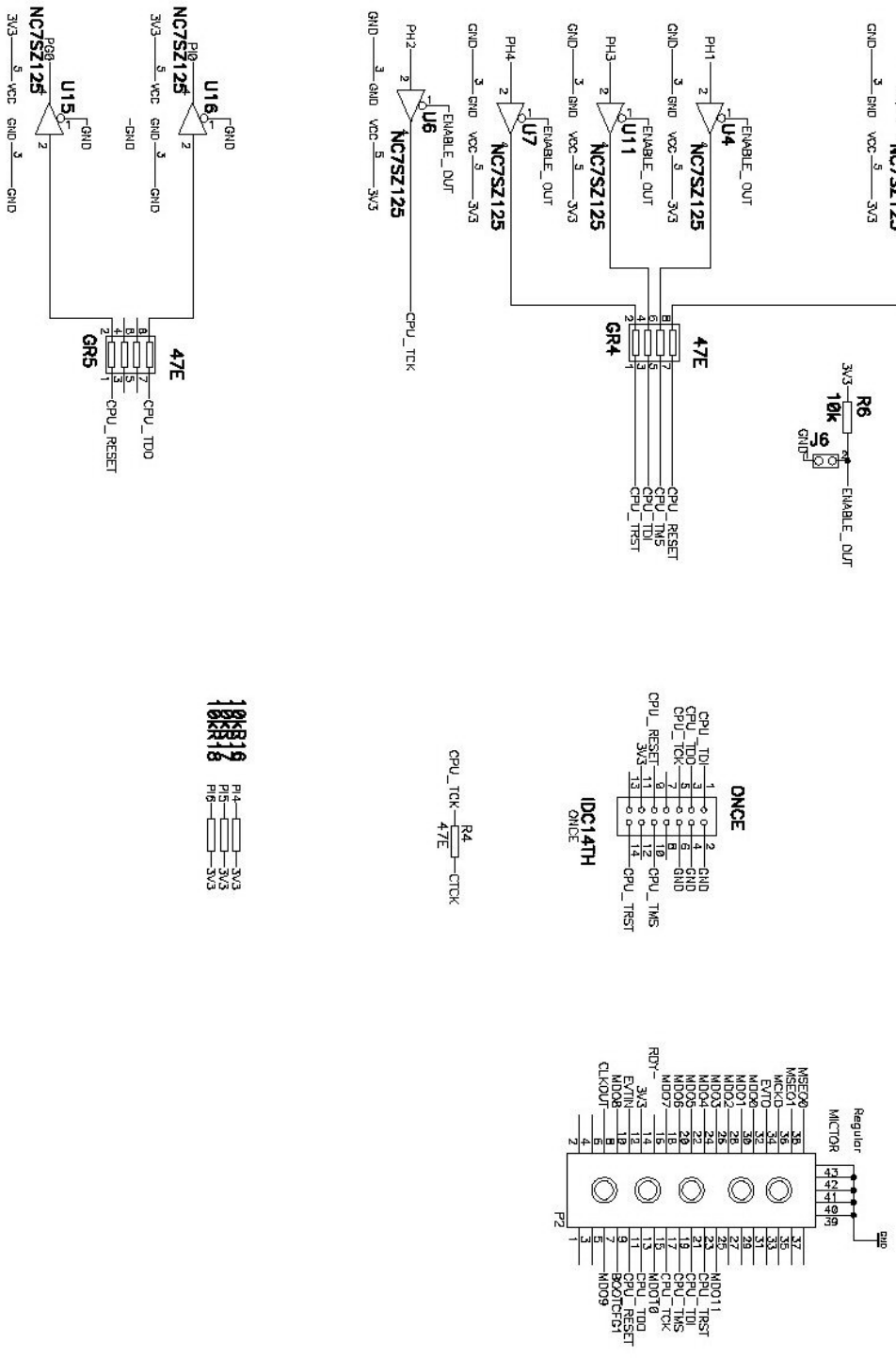
Note: A designation on *Figure 4* stands for A1 designation on the above ITMPC5566 view, B stands for B1, AF stands for AF1 etc.

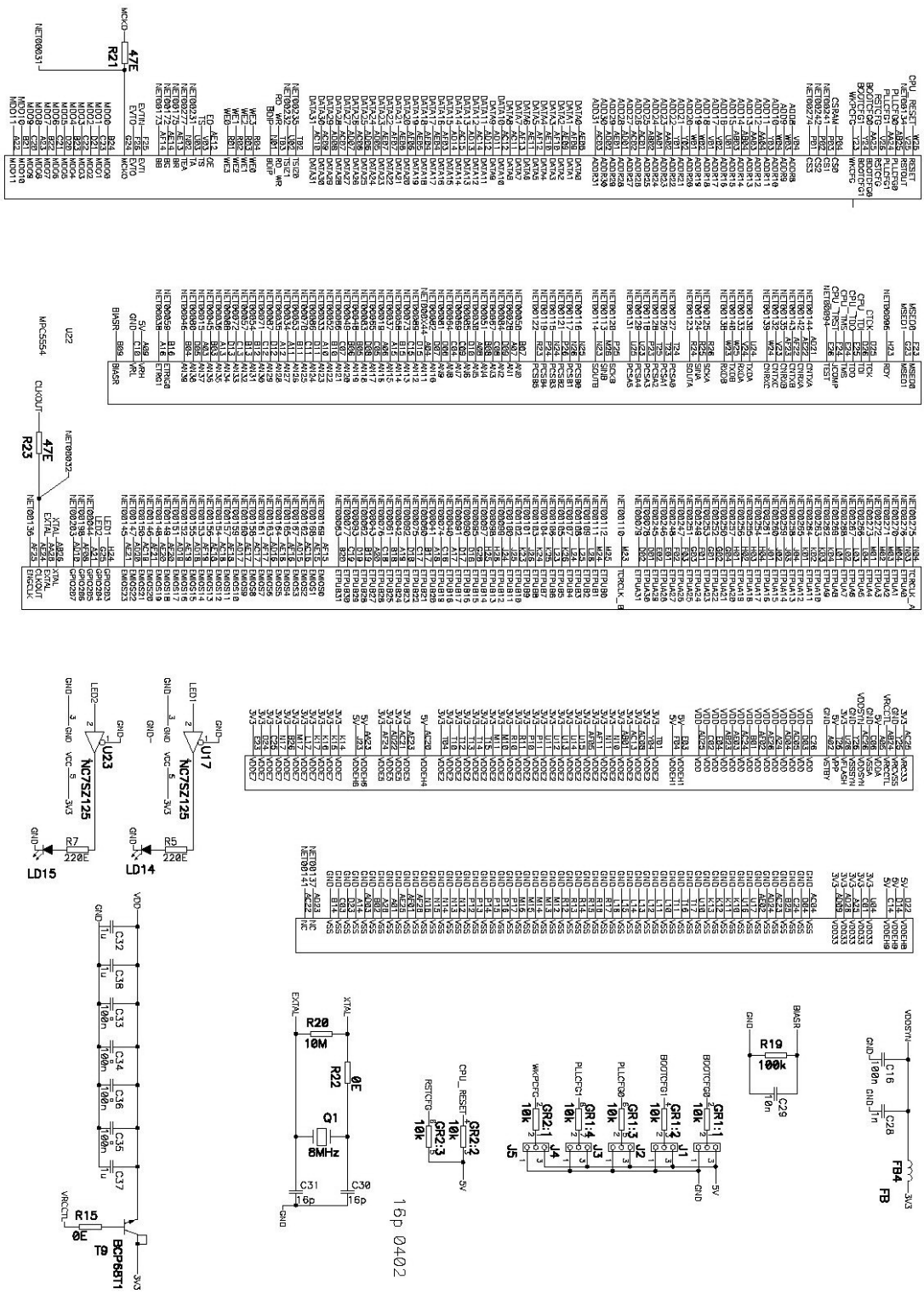
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	V_{SS}	V_{STBY}	AN37	AN11	V_{DDA}	AN16	AN1	AN5	VRH	AN23	AN27	AN28	AN35	V_{SS}	AN15	ETRG1	ETPUB18	ETPUB20	ETPUB24	ETPUB27	GPIO 205	MDO11	MDO8	V_{DD}	V_{DD33}	V_{SS}	A
B	V_{DD}	V_{SS}	AN36	AN39	AN19	AN20	AN0	AN4	BIASR	AN22	AN26	AN31	AN32	V_{SS}	AN14	ETRIG0	ETPUB21	ETPUB25	ETPUB28	ETPUB31	MDO10	MDO7	MDO4	MDO0	V_{SS}	V_{DDE7}	B
C	V_{DD33}	V_{DD}	V_{SS}	AN8	AN17	V_{SSA}	AN21	AN3	AN7	VRL	AN25	AN30	AN33	V_{DDEH9}	AN13	ETPUB19	ETPUB22	ETPUB26	ETPUB30	MDO9	MDO6	MDO3	MDO1	V_{SS}	V_{DDE7}	V_{DD}	C
D	ETPUA30	ETPUA31	V_{DD}	V_{SS}	AN38	AN9	AN10	AN18	AN2	AN6	AN24	AN29	AN34	V_{DDEH9}	AN12	ETPUB16	ETPUB17	ETPUB23	ETPUB29	MDO5	MDO2	V_{DDEH3}	V_{SS}	V_{DDE7}	TCK	TDI	D
E	ETPUA28	ETPUA29	V_{DDEH1}	V_{DD}	(As viewed from the top of the package)																		V_{DDE7}	TMS	TDO	$\overline{TEST}$	E
F	ETPUA24	ETPUA27	ETPUA26	V_{DDEH1}																			$\overline{MSEO0}$	JCOMP	EVTI	$\overline{EVTO}$	F
G	ETPUA23	ETPUA22	ETPUA25	ETPUA21																			$\overline{MSEO1}$	MCKO	GPIO204	ETPUB15	G
H	ETPUA20	ETPUA19	ETPUA18	ETPUA17																			$\overline{RDY}$	GPIO203	ETPUB14	ETPUB13	H
J	ETPUA16	ETPUA15	ETPUA14	ETPUA13																			V_{DDEH6}	ETPUB12	ETPUB11	ETPUB9	J
K	ETPUA12	ETPUA11	ETPUA10	ETPUA9																			ETPUB10	ETPUB8	ETPUB7	ETPUB5	K
L	ETPUA8	ETPUA7	ETPUA6	ETPUA5																			ETPUB6	ETPUB4	ETPUB3	ETPUB2	L
M	ETPUA4	ETPUA3	ETPUA2	ETPUA1																			TCRCLKB	ETPUB1	ETPUB0	SINB	M
N	$\overline{BDIP}$	$\overline{TEA}$	ETPUA0	TCRCLKA																			SOUTB	PCSB3	PCSB0	PCSB1	N
P	$\overline{CS3}$	$\overline{CS2}$	$\overline{CS1}$	$\overline{CS0}$																			PCSA3	PCSB4	SCKB	PCSB2	P
R	$\overline{WE3}$	$\overline{WE2}$	$\overline{WE1}$	$\overline{WE0}$																			PCSB5	SOUTA	SINA	SCKA	R
T	V_{DDE1}	TSIZ0	RD_$\overline{WR}$	V_{DDE2}																			PCSA1	PCSA0	PCSA2	V_{PP}	T
U	ADDR16	TSIZ1	$\overline{TA}$	V_{DD33}																			PCSA4	TXDA	PCSA5	V_{FLASH}	U
V	ADDR18	ADDR17	$\overline{TS}$	ADDR8																			CNTXC	RXDA	$\overline{RSTOUT}$	$\overline{RSTCFG}$	V
W	ADDR20	ADDR19	ADDR9	ADDR10																			RXDB	CNRXC	TXDB	$\overline{RESET}$	W
Y	ADDR22	ADDR21	ADDR11	V_{DDE2}																			WKCFG	BOOTCFG1	V_{RCVSS}	V_{SSSYN}	Y
AA	ADDR24	ADDR23	ADDR13	ADDR12																			V_{DDEH6}	PLLCFG1	BOOTCFG0	EXTAL	AA
AB	V_{DDE2}	ADDR25	ADDR15	ADDR14																			V_{DD}	V_{RCCTL}	PLLCFG0	XTAL	AB
AC	ADDR26	ADDR27	ADDR31	V_{SS}	V_{DD}	DATA26	DATA28	V_{DDE2}	DATA30	DATA31	DATA8	DATA10	V_{DDE2}	DATA12	DATA14	EMIOS2	EMIOS8	EMIOS12	EMIOS21	V_{DDEH4}	V_{DDE5}	NC	V_{SS}	V_{DD}	V_{RC33}	V_{DDSYN}	AC
AD	ADDR28	ADDR30	V_{SS}	V_{DD}	DATA24	DATA25	DATA27	DATA29	V_{DD33}	GPIO 207	DATA9	DATA11	DATA13	DATA15	EMIOS3	EMIOS6	EMIOS10	EMIOS15	EMIOS17	EMIOS22	CNTXA	V_{DDE5}	NC	V_{SS}	V_{DD}	V_{DD33}	AD
AE	ADDR29	V_{SS}	V_{DD}	DATA17	DATA19	DATA21	DATA33	DATA0	DATA2	DATA4	DATA6	$\overline{OE}$	$\overline{BR}$	$\overline{BG}$	EMIOS1	EMIOS5	EMIOS9	EMIOS13	EMIOS16	EMIOS19	EMIOS23	CNRXA	V_{DDE5}	CLKOUT	V_{SS}	V_{DD}	AE
AF	V_{SS}	V_{DD}	DATA16	DATA18	V_{DDE2}	DATA20	DATA22	GPIO 206	DATA1	DATA3	V_{DDE2}	DATA5	DATA7	$\overline{BB}$	EMIOS0	EMIOS4	EMIOS7	EMIOS11	EMIOS14	EMIOS18	EMIOS20	CNTXB	CNRXB	V_{DDE5}	ENGCLK	V_{SS}	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Figure 4: Expansion connector

Schematic

Note: On-board integrated JTAG debugger is not part of the schematic.




R21
47E
R23
47E
U22
MPC5554
U23
NC7SZ125
U17
NC7SZ125
LD15
LD14
R20
10M
R22
0E
Q1
8MHz
C31
16p
C30
16p
R15
0E
T9
BCP68T1
R19
100k
C29
10n
C16
100n
C28
1n
FB4
FB
J1
J2
J3
J4
J5
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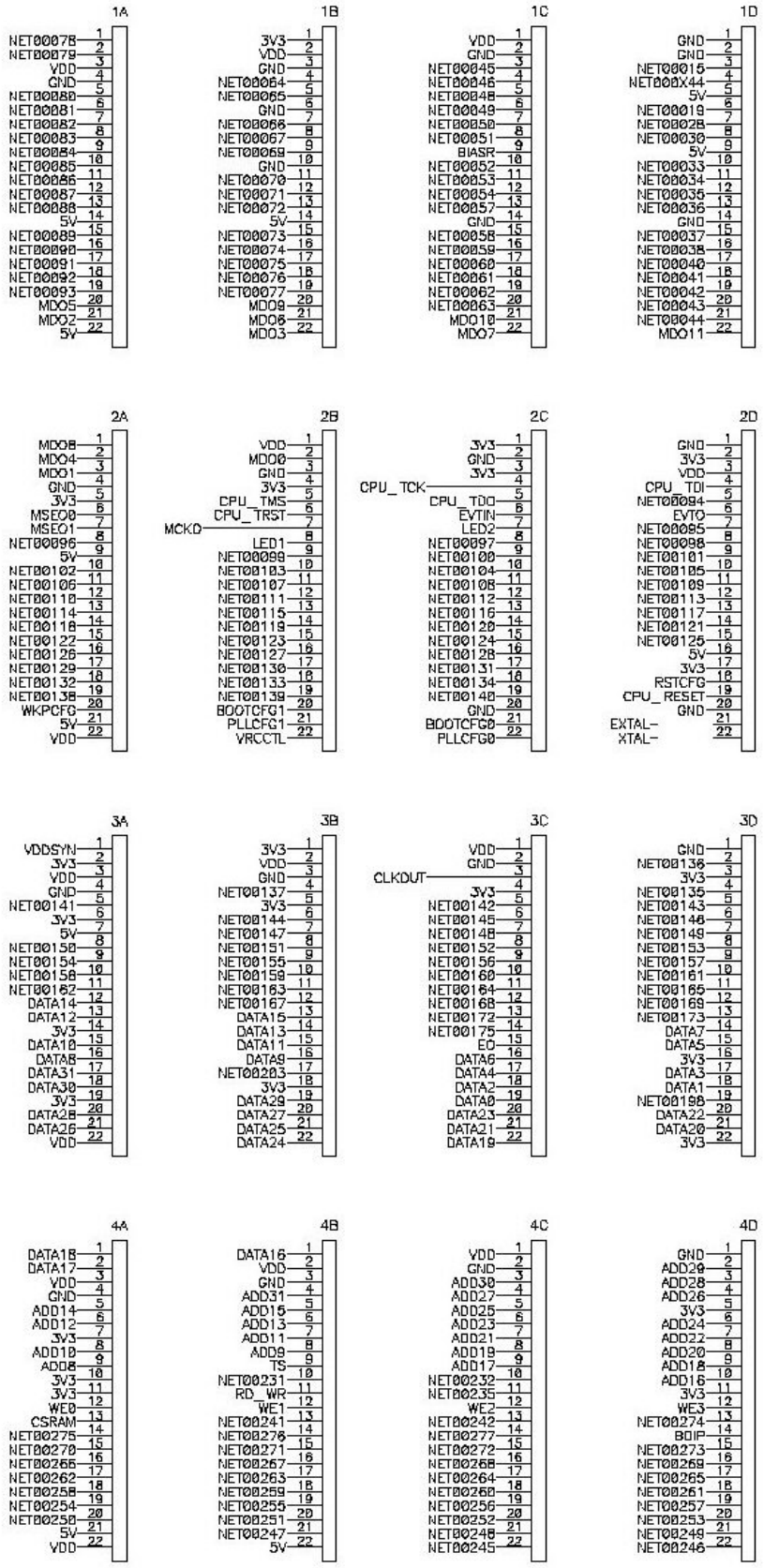
GR2:1
GR2:2
GR2:3
10k
16p 0402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NET00078 1
NET00079 2
VDD 3
GND 4
NET00080 5
NET00081 6
NET00082 7
NET00083 8
NET00084 9
NET00085 10
NET00086 11
NET00087 12
NET00088 13
5V 14
NET00089 15
NET00090 16
NET00091 17
NET00092 18
NET00093 19
MDO5 20
MDO2 21
5V 22
1B
3V3 1
VDD 2
GND 3
NET00064 4
NET00065 5
GND 6
NET00066 7
NET00067 8
NET00069 9
GND 10
NET00070 11
NET00071 12
NET00072 13
5V 14
NET00073 15
NET00074 16
NET00075 17
NET00076 18
NET00077 19
MDO9 20
MDO6 21
MDO3 22
1C
VDD 1
GND 2
NET00045 3
NET00046 4
NET00048 5
NET00049 6
NET00050 7
NET00051 8
BIASR 9
NET00052 10
NET00053 11
NET00054 12
NET00057 13
GND 14
NET00058 15
NET00059 16
NET00060 17
NET00061 18
NET00062 19
NET00063 20
MDO10 21
MDO7 22
1D
GND 1
GND 2
NET00015 3
NET00X44 4
5V 5
NET00019 6
NET00028 7
NET00030 8
5V 9
NET00033 10
NET00034 11
NET00035 12
NET00036 13
GND 14
NET00037 15
NET00038 16
NET00040 17
NET00041 18
NET00042 19
NET00043 20
NET00044 21
MDO11 22
2A
MDO8 1
MDO4 2
MDO1 3
GND 4
3V3 5
MSEO0 6
MSEO1 7
NET00096 8
5V 9
NET00102 10
NET00106 11
NET00110 12
NET00114 13
NET00118 14
NET00122 15
NET00126 16
NET00129 17
NET00132 18
NET00138 19
WKPCFG 20
5V 21
VDD 22
2B
VDD 1
MDO0 2
GND 3
3V3 4
CPU_TMS 5
CPU_TRST 6
MCKO 7
LED1 8
NET00099 9
NET00103 10
NET00107 11
NET00111 12
NET00115 13
NET00119 14
NET00123 15
NET00127 16
NET00130 17
NET00133 18
NET00139 19
BOOTCFG1 20
PLLCFG1 21
VRCCTL 22
2C
3V3 1
GND 2
3V3 3
CPU_TCK 4
CPU_TDO 5
EVTIN 6
LED2 7
NET00097 8
NET00100 9
NET00104 10
NET00108 11
NET00112 12
NET00116 13
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NET00124 15
NET00128 16
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NET00134 18
NET00140 19
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BOOTCFG0 21
PLLCFG0 22
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VDD 3
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EVTO 6
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NET00098 8
NET00101 9
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NET00117 13
NET00121 14
NET00125 15
5V 16
3V3 17
RSTCFG 18
CPU_RESET 19
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EXTAL 21
XTAL 22
3A
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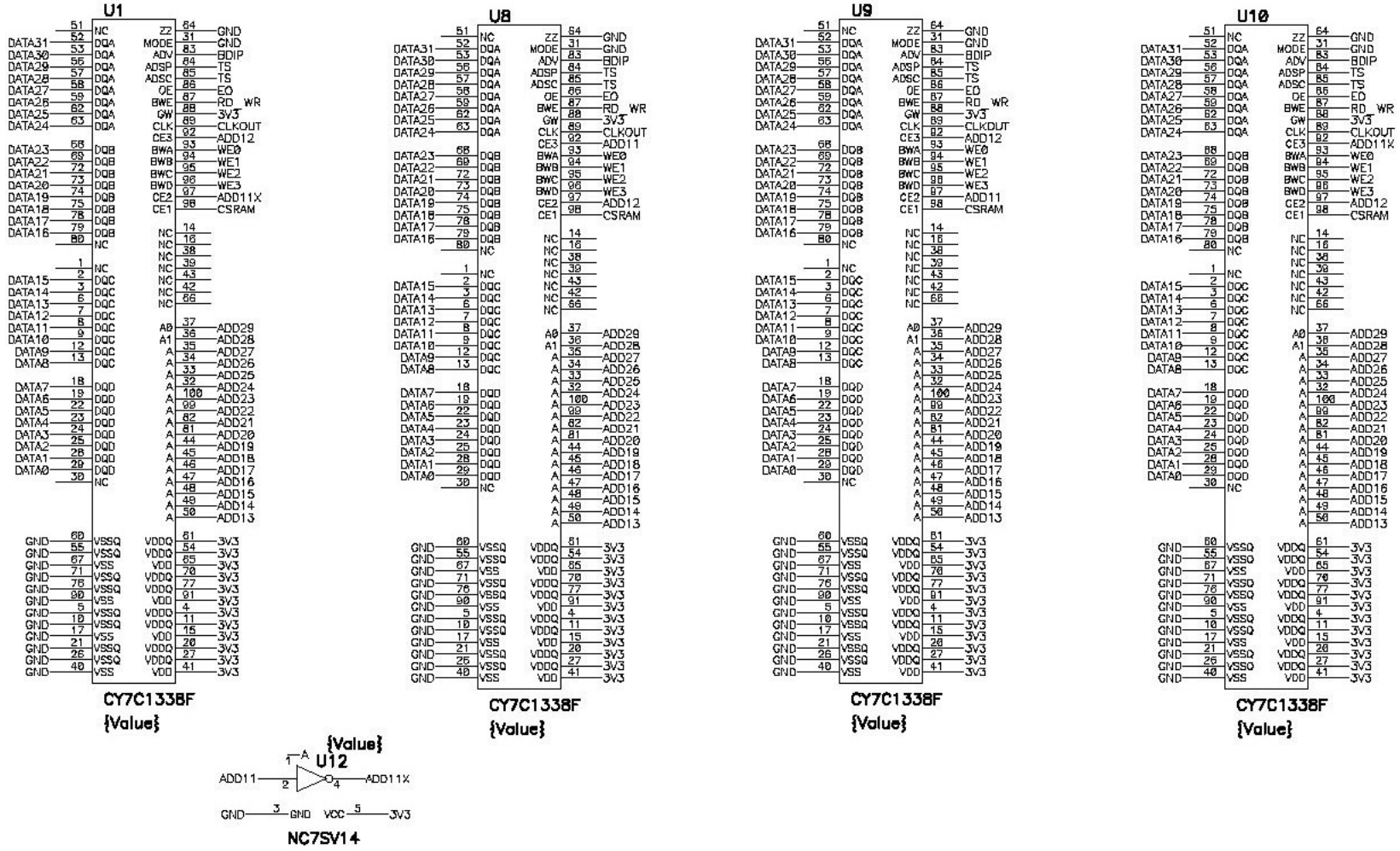
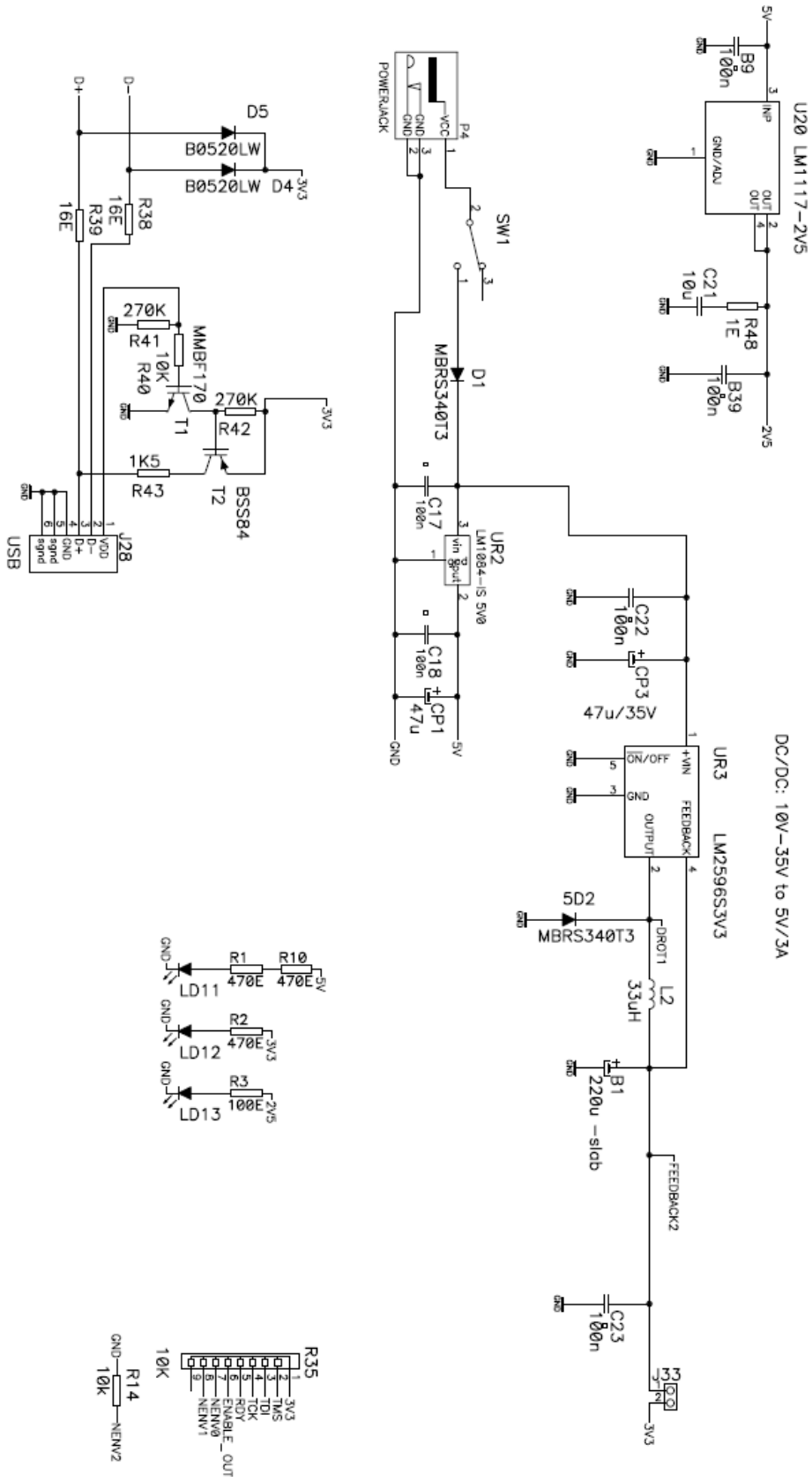
3V3 2
VDD 3
GND 4
NET00141 5
3V3 6
5V 7
NET00150 8
NET00154 9
NET00158 10
NET00162 11
DATA14 12
DATA12 13
3V3 14
DATA10 15
DATA8 16
DATA31 17
DATA30 18
3V3 19
DATA28 20
DATA26 21
VDD 22
3B
3V3 1
VDD 2
GND 3
NET00137 4
3V3 5
NET00144 6
NET00147 7
NET00151 8
NET00155 9
NET00159 10
NET00163 11
NET00167 12
DATA15 13
DATA13 14
DATA11 15
DATA9 16
NET00203 17
3V3 18
DATA29 19
DATA27 20
DATA25 21
DATA24 22
3C
VDD 1
GND 2
CLKOUT 3
3V3 4
NET00142 5
NET00145 6
NET00148 7
NET00152 8
NET00156 9
NET00160 10
NET00164 11
NET00168 12
NET00172 13
NET00175 14
EO 15
DATA6 16
DATA4 17
DATA2 18
DATA0 19
DATA23 20
DATA21 21
DATA19 22
3D
GND 1
NET00136 2
3V3 3
NET00135 4
NET00143 5
NET00146 6
NET00149 7
NET00153 8
NET00157 9
NET00161 10
NET00165 11
NET00169 12
NET00173 13
DATA7 14
DATA5 15
3V3 16
DATA3 17
DATA1 18
NET00198 19
DATA22 20
DATA20 21
3V3 22
4A
DATA18 1
DATA17 2
VDD 3
GND 4
ADD14 5
ADD12 6
3V3 7
ADD10 8
ADD8 9
3V3 10
3V3 11
WE0 12
CSRAM 13
NET00275 14
NET00270 15
NET00266 16
NET00262 17
NET00258 18
NET00254 19
NET00250 20
5V 21
VDD 22
4B
DATA16 1
VDD 2
GND 3
ADD31 4
ADD15 5
ADD13 6
ADD11 7
ADD9 8
TS 9
NET00231 10
RD_WR 11
WE1 12
NET00241 13
NET00276 14
NET00271 15
NET00267 16
NET00263 17
NET00259 18
NET00255 19
NET00251 20
NET00247 21
5V 22
4C
VDD 1
GND 2
ADD30 3
ADD27 4
ADD25 5
ADD23 6
ADD21 7
ADD19 8
ADD17 9
NET00232 10
NET00235 11
WE2 12
NET00242 13
NET00277 14
NET00272 15
NET00268 16
NET00264 17
NET00260 18
NET00256 19
NET00252 20
NET00248 21
NET00245 22
4D
GND 1
ADD29 2
ADD28 3
ADD26 4
3V3 5
ADD24 6
ADD22 7
ADD20 8
ADD18 9
ADD16 10
3V3 11
WE3 12
NET00274 13
BOIP 14
NET00273 15
NET00269 16
NET00265 17
NET00261 18
NET00257 19
NET00253 20
NET00249 21
NET00246 22




U20 LM1117-2V5
B9 100n
C21 10u
R48 1E
B39 100n
POWERJACK
SW1
D1 MBRS340T3
C17 100n
C18 100n
UR2 LM1084-IS 5V0
CP1 47u
C22 100n
CP3 47u/35V
UR3 LM2596S3V3
DC/DC: 10V-35V to 5V/3A
5D2 MBRS340T3
L2 33uH
B1 220u -slab
FEEDBACK2
C23 100n
D5 B0520LW
D4 B0520LW
R38 16E
R39 16E
270K R41
10K R40
MMBF170 T1
270K R42
1K5 R43
BSS84 T2
J28 USB
LD11 R1 470E R10 470E
LD12 R2 470E
LD13 R3 100E
R35 10K
R14 10k

Notes: