ARM Cortex On-Chip Trace

Contents

1 Trace

Cortex-based CPUs can contain none, one or more on-chip trace units which can all simultaneously be active and generate trace output. Some significant changes were introduced to the system architecture to allow for multiple trace streams to be output and captured. Cortex CPUs internally implement CoreSight component architecture which provides a way to output multiple trace streams over a single trace port.

Cortex-based CPUs can come equipped with no, one or more trace modules of different types:

ITM	- Instrumentation Trace Macrocell (software instrumentation)
DWT	- Data Watchpoint and Trace (DWT hardware event trace)
ETM	- Embedded Trace Macrocell (instruction and/or data trace)
PTM	- Program Trace Macrocell (instruction trace)
HTM	- AMBA AHB Trace Macrocell (address and data trace of AHB bus)

ITM and DWT are common on Cortex-M CPUs but not on Cortex-R or Cortex-A profiles. ITM provides “printf”-like trace ability using stimulus ports (memory mapped) to which target application can perform memory writes whose information is then output in a form of a trace packet in the ITM/DWT trace stream. DWT provides a low bandwidth focused data trace using comparators to detect memory accesses and then generate trace packets with information about memory accesses.

ETM trace module comes in a couple of versions. Cortex-M ETM variants usually don’t feature data trace and own comparators. Cortex A/R ETM is usually fully featured.

PTM is mostly implemented on high performance Cortex-A devices.

HTM is an AMBA bus trace cell which can be found on some higher-end Cortex-M based CPUs. HTM provides full data trace capability to complement the Cortex-M ETM which offers only program flow trace.

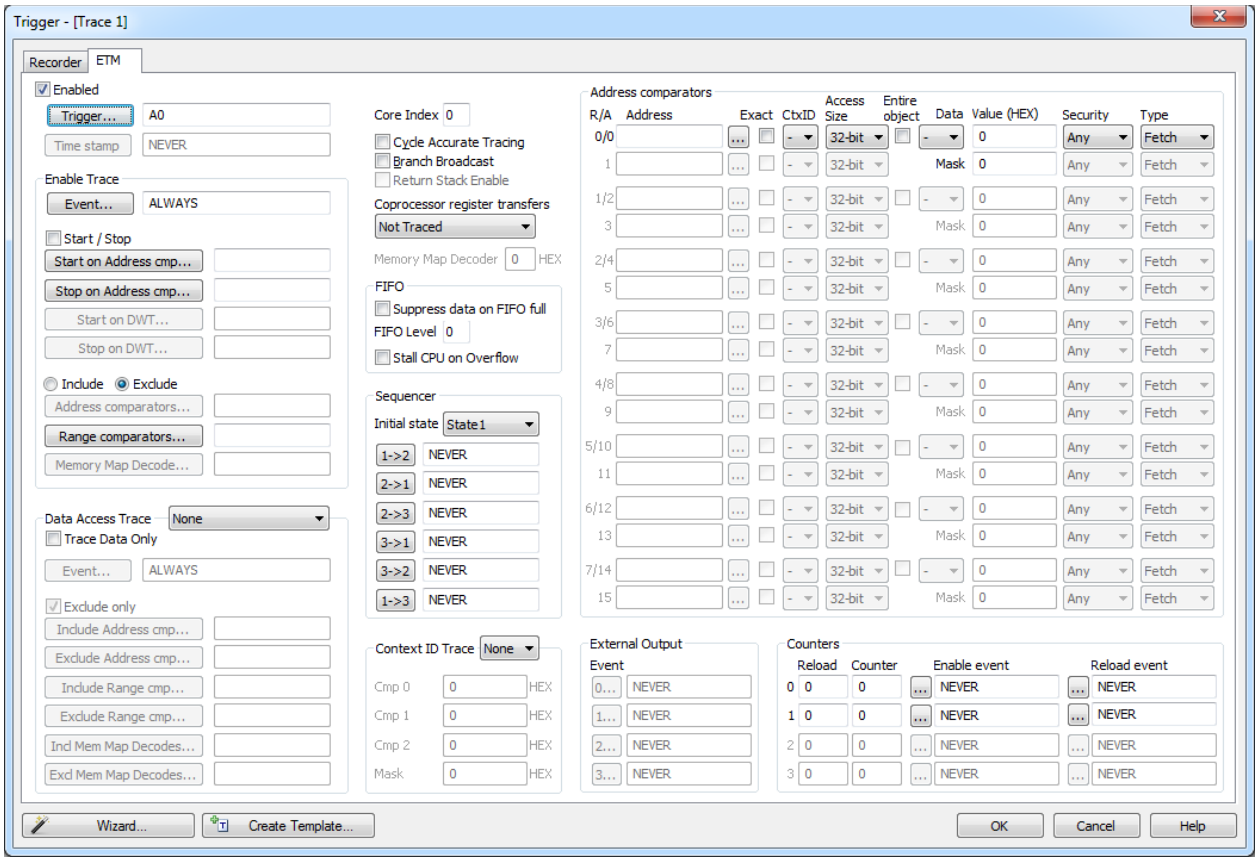
Each of different trace units also incorporates its own triggering system which can make for a quite complex trigger configuration on CPUs with multiple trace units on-board.

All trace sources on Cortex based CPUs output trace information in a byte oriented stream protocol and this is the key factor that allows multiple trace sources to be output over a single trace port in a merged trace stream which is then recorded by iSYSTEM trace hardware.

1.1 Embedded Trace Macrocell (ETM)

ETM is a trace source component which outputs information stream about program execution and data accesses. It is common to all Cortex profiles (A, R and M).

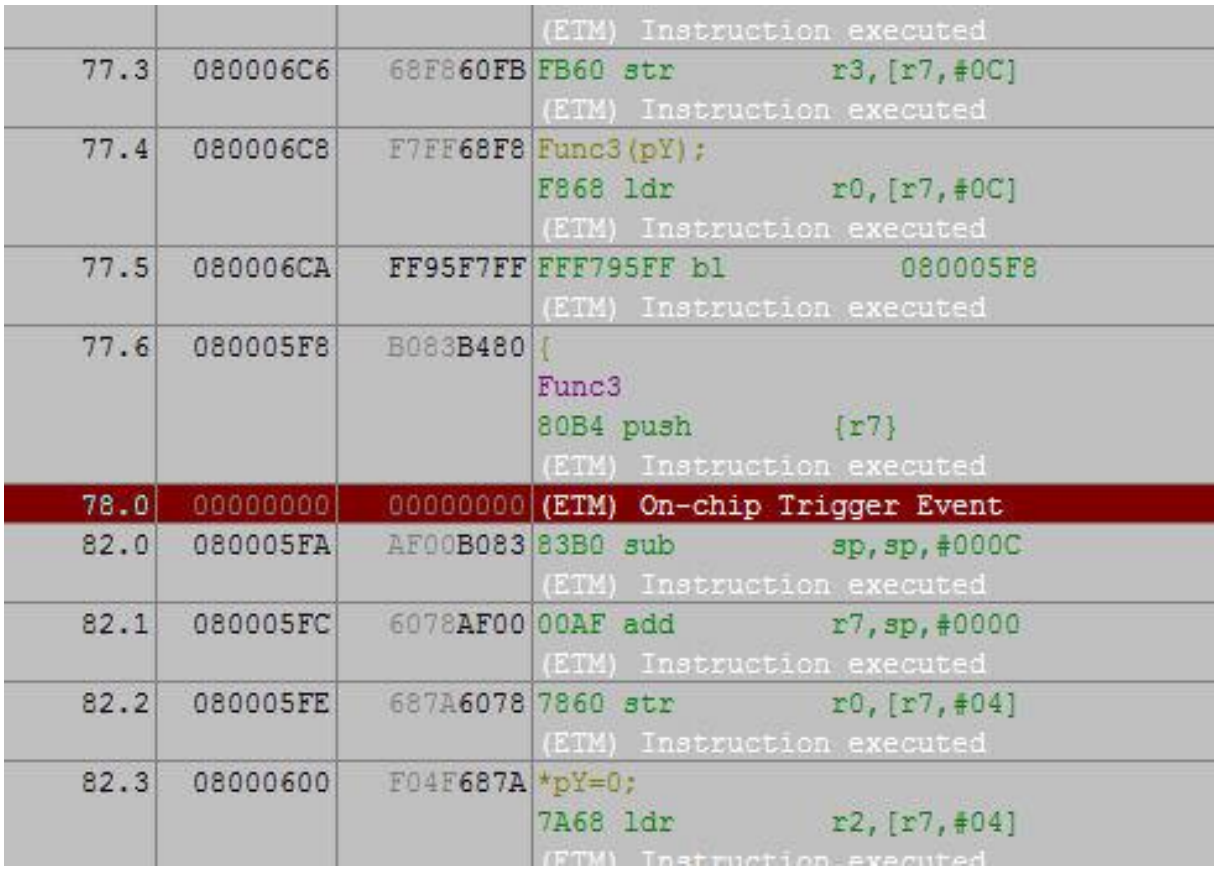
winIDEA provides a dialog for ETM component configuration within Analyzer trigger configuration:



ETM dialog

Dialog is made per ETM architecture specification. Note that specific ETM implementation defines the available functionality and resources. Consult specific ETM implementation documentation for detailed information about available functionality and resources. In winIDEA the parts that are not available on ETM for selected CPU are disabled and cannot be configured in dialog.

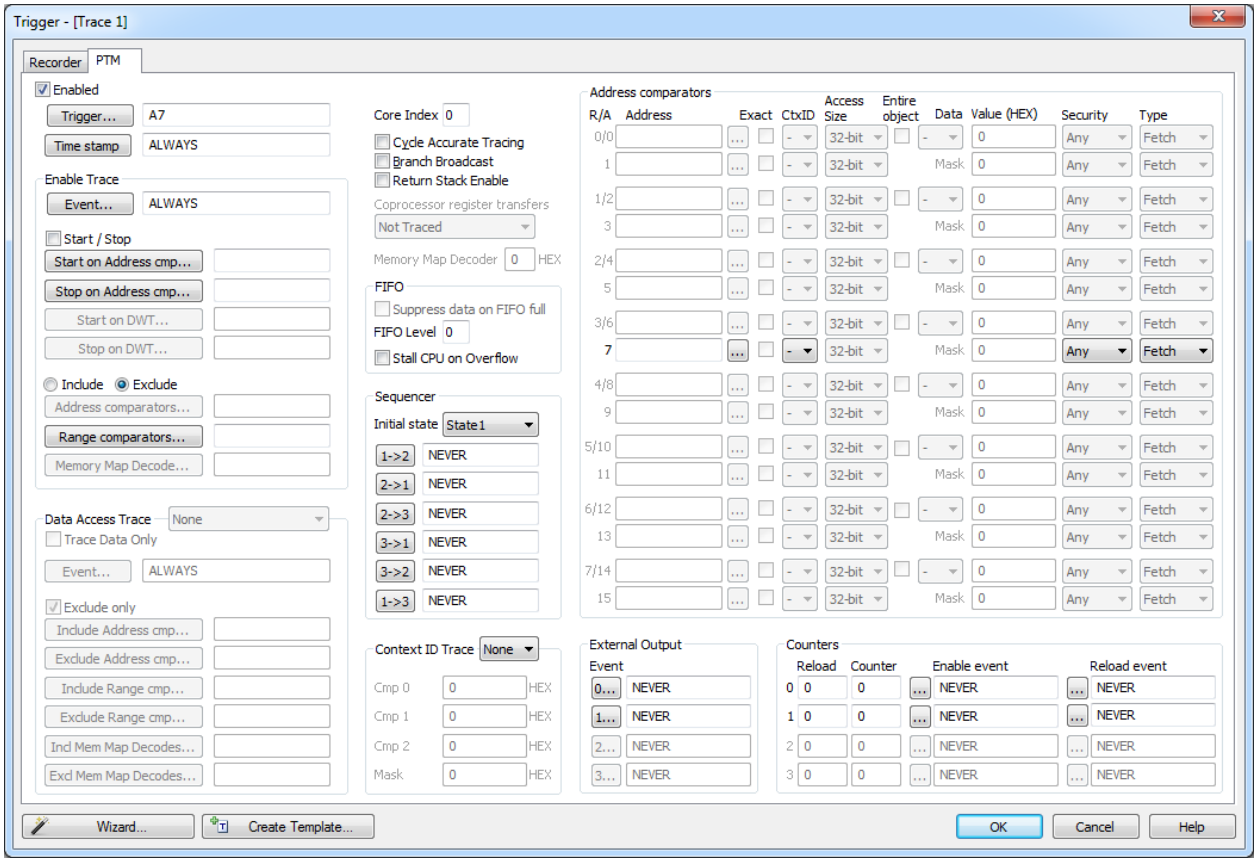
Use **'Wizard…'** for easier configuration of common trace scenarios.



Example of ETM output stream in Trace window

1.2 Program Trace Macrocell (PTM)

Newer Cortex A devices features PTM instead of ETM. winIDEA trace configuration dialog provides a dialog for PTM component configuration. Note that PTM doesn't feature data trace capabilities.

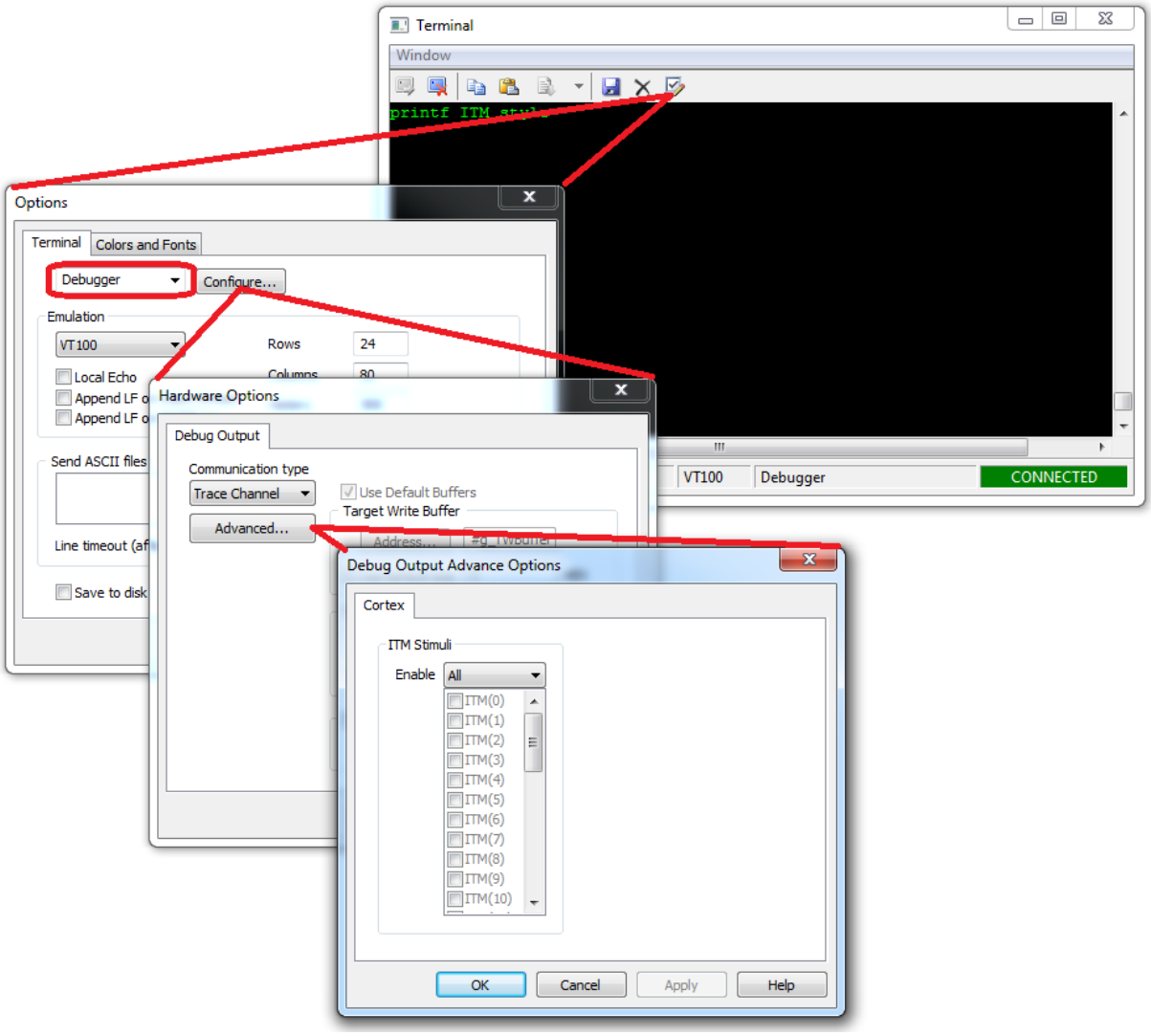


PTM dialog

Parts of dialog are disabled according to the capabilities of selected CPU.

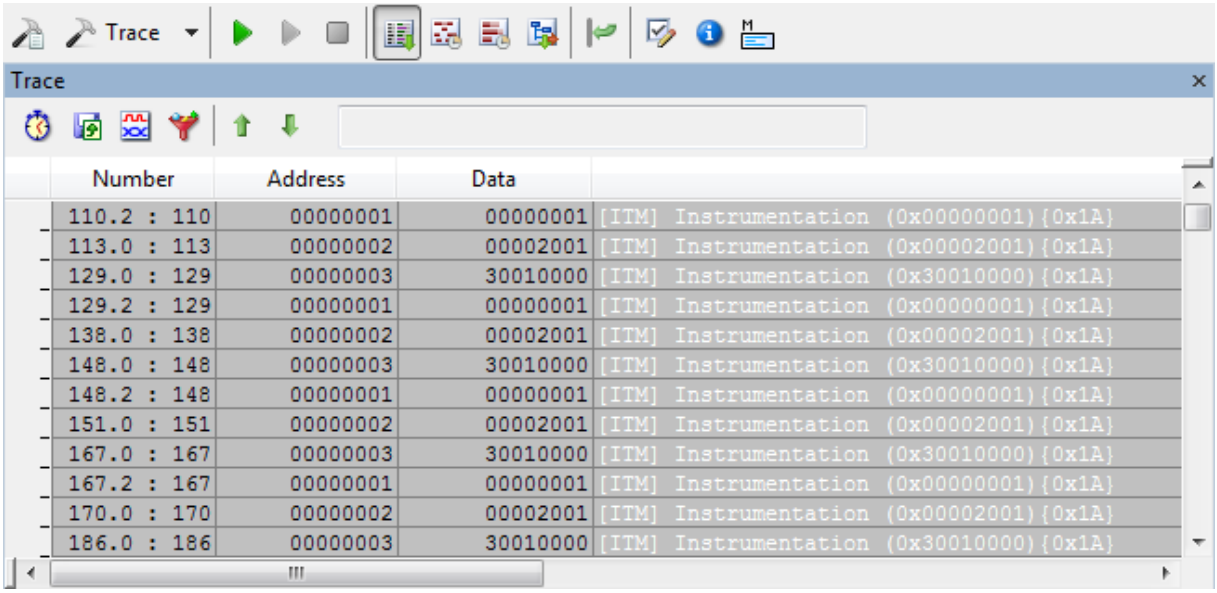
1.3 Instrumentation Trace Macrocell (ITM)

ITM module enables software instrumentation in the target application (same concept as with *printf*). Software instrumentation is performed by the target application writing application specific values into a series of ITM stimulus port registers which cause trace messages to be output over the trace port. winIDEA displays ITM output either in Trace window or terminal window. ITM with DWT is usually featured on Cortex-M devices.



ITM terminal example usage and configuration

In Trace window the stimulus register ID is shown in Address column and data written to it in Data column.



ITM results in the trace window

ITM module configuration is combined in a dialog with DWT configuration (see Data Watchpoint and Trace for more information).

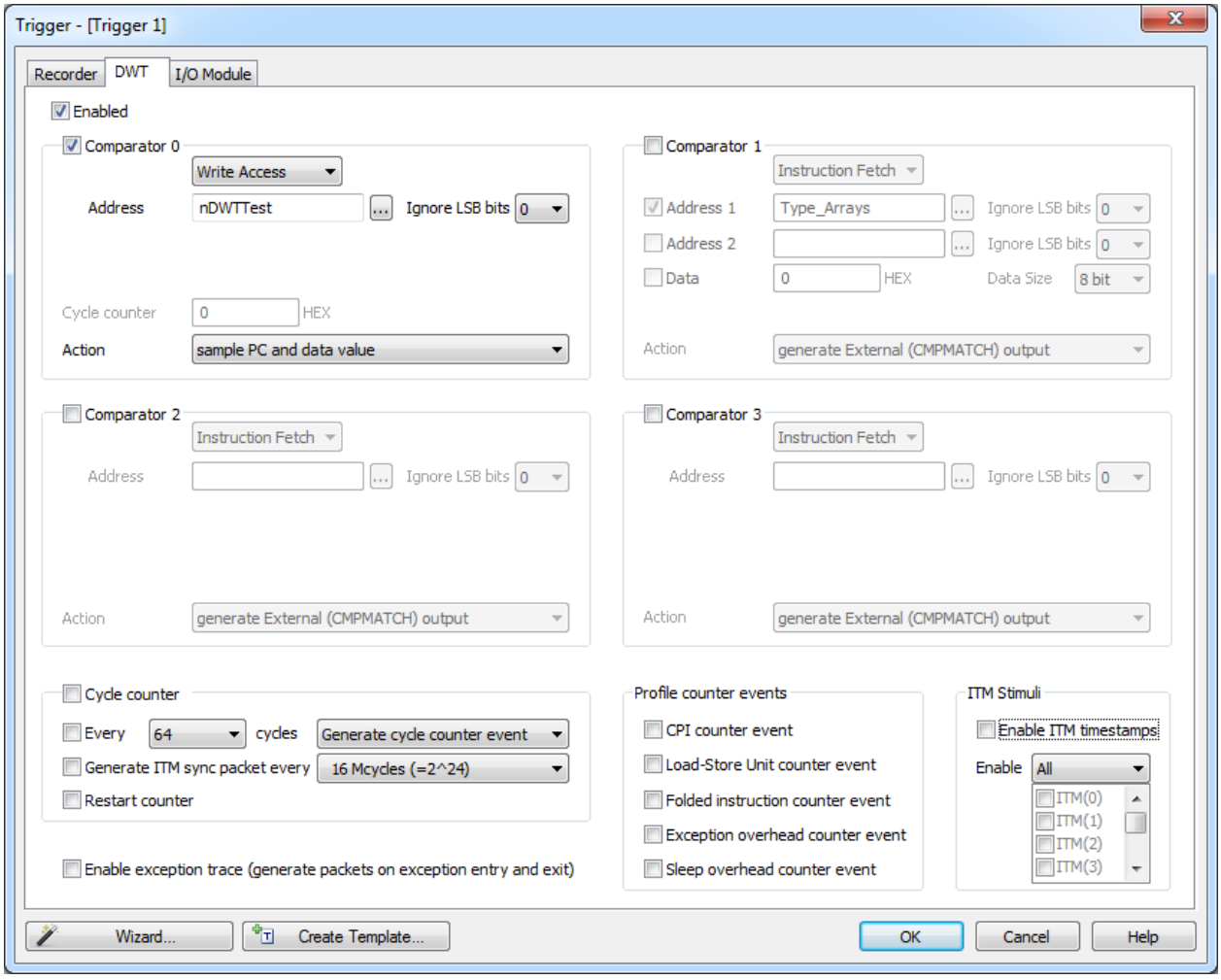
1.4 Data Watchpoint and Trace (DWT)

DWT module provides means for generating various hardware trace events which are user configurable like hardware access breakpoints (see Access Breakpoints for more information). This is due to the same hardware comparators used for hardware access breakpoints and trace event generation.

Note: If DWT hardware comparators are used for access breakpoint operation, then they cannot be used for trace event generation at the same time.

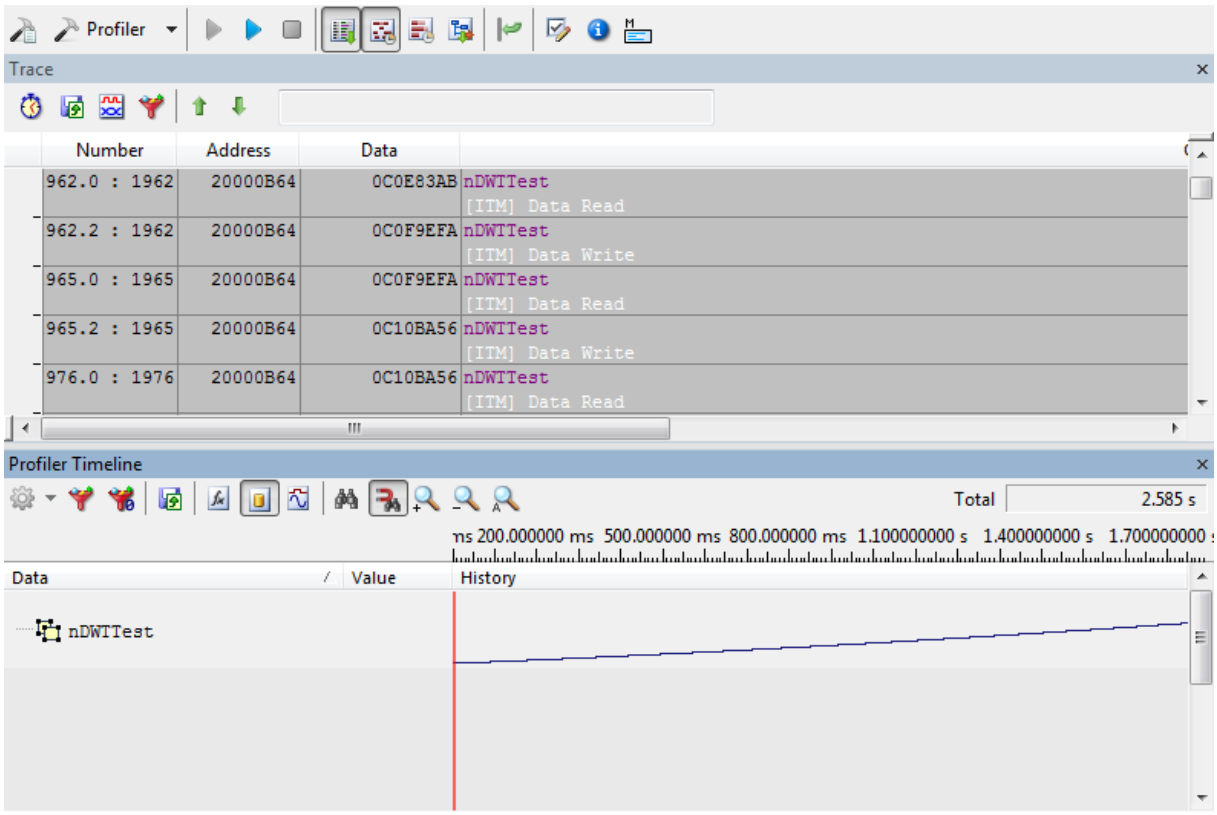
DWT with ITM is usually featured on Cortex-M devices.

winIDEA provides a dialog for DWT configuration. It is combined with ITM configuration because the two modules are usaully featured together. Not all possible options might be configurable. The set of configurable options is defined by device implementation.



DWT hardware event generation and ITM configuration

Note that access type distinction (read, write, read or write) for the DWT comparators is not supported on every device. Consult device documentation for more information on explicit access distinction.



DWT Trace and Profiler results